SUPER FAMICOM

CONTENTS

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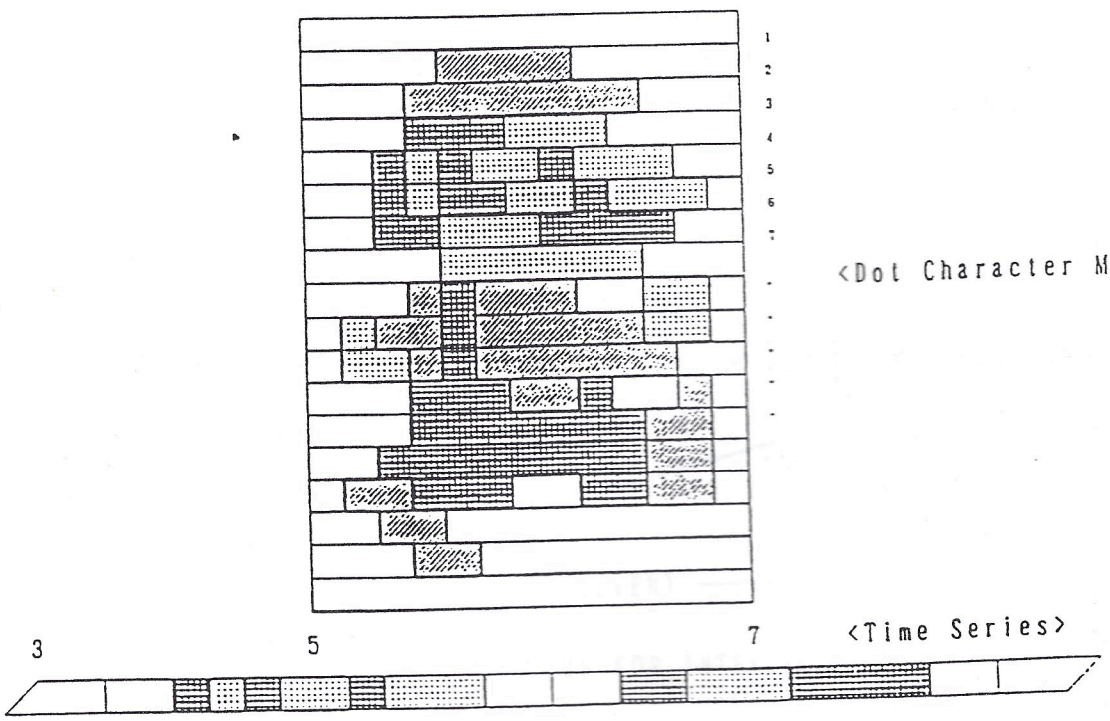
§ 1 INTRODUCTION

Thank you for your interest in developing software for the Super Famicom (SFX). We would like to explain briefly the basic information concerning the home television system. Even if you have been engaged in developing software for the Family Computer (Famicom), please read once for your review.

1. PICTURE IMAGE ON TELEVISION SYSTEM

The picture on a color television system consists of 525 holizontal lines with each line having the color stripes. The broadcasting station breakdowns the picture into lines as shown on Fig.1.
The odd number lines are converted to electric signal from the top to the bottom on the screen, and then, the remaining even number lines will be converted from the top to the bottom in the same way.
The method which traces every two lines is called the "INTERLACE".
For the television system, the electric signal which has been sent is converted to the light signal, and it will traces on the TV screen according to the order above.
The light traces on the screen is called the "scanning", and the period for scanning the odd number line is called the "1st field", and the period for scanning the even number line is called the "2nd field".
A period for scanning on the screen is called "one frame", and this is a period combined of the 1st field and the 2nd field in case of the TV broadcasting. Because of 1/60 sec (one field) and 1/30 sec (one frame), a certain portion on the screen is radiated only every 1/30 sec. However, because of the afterimage of human eyes and the afterglow of the CRT, it does not seem to flicker.



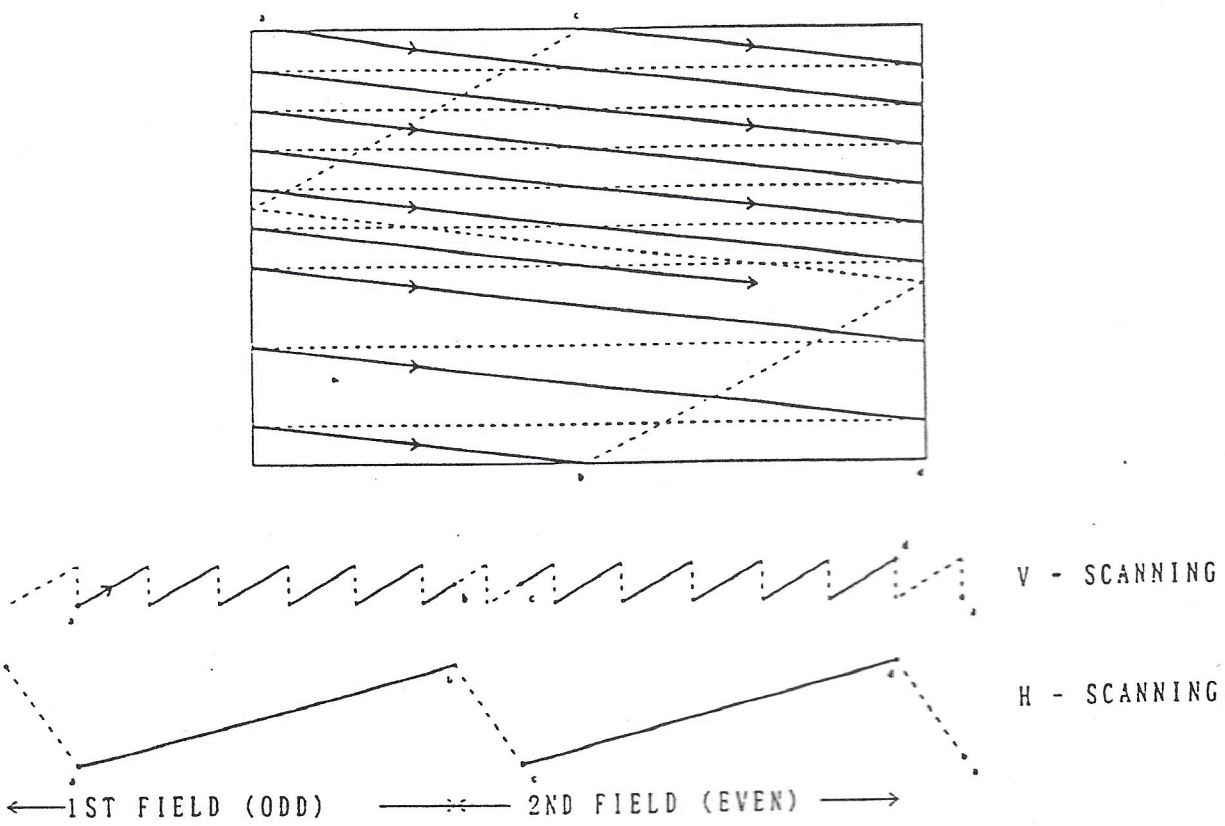
[Fig.1] Scanning Process

2. SFX DISPLAY

The picture display on the SFX has two modes. One is the Interlace mode based on the television system, and the other is Non-Interlace mode which one frame takes 1/60 second. In the Non-Interlace mode, same position is scanned every field, therefore, lines of a frame are only 262, which means, half of the Interlace mode.
Furthermore, there seems to be no flickering compared to the Interlace mode, since one point on the screen radiates every 1/60 second.

3. BLANK

The screen is scanned from the left to the right and from the top to the bottom on the screen (See Fig.2). After scanning from the left to the right, it sould move back to the left without radiating, and after scanning from the top to the bottom, it should move back to the top without radiating.
It takes a certain amount of time for the scanning.
The former is called H-Blank, and the later is called V-blank.
The Famicom and the SFX use this Blank efficiently to display various movement of the characters.



[Fig.2] SCANNING PATTERN FOR INTERLACE

§ 2 OBJ (OBJECT)

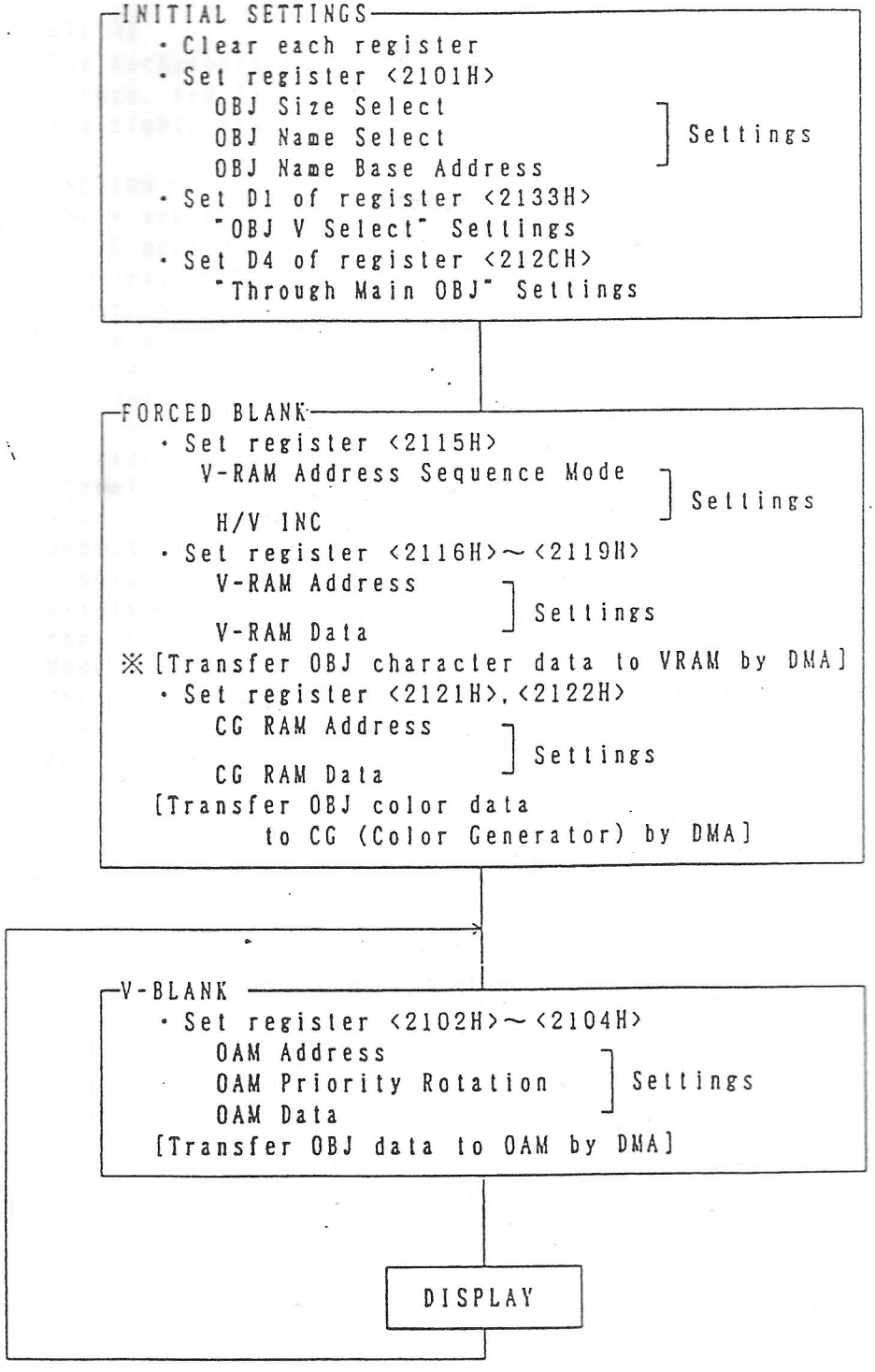
1. OUTLINE

This function can display the Object on a certain position on the screen. The characters, such as the UFO or the missile of a space game, look like they are active in moving this position.
If the character's picture is replaced at the same time the point is moved, animation effects can occur, such as "Mario" character looking like it's walking.

2. FUNCTION

The maximum number of OBJs that can be displayed on the screen is 128 and there are four sizes. However, two sizes can be selected in one frame and one size should be selected for each OBJ.
There are 8 color palettes in the whole OBJs, and one palette should be selected for each OBJ. One color palette has 16 color codes out of 32768 colors, therefore, each OBJ is the picture drawn by 16 colors. Each 128 OBJs has its own priority order, which will decide the display priority if 2 or more OBJs are overlapped.
Furthermore, there is the Flip function of up-down, and left-right, BG priority order and the priority order shifting function.

3. SETTING EXAMPLE



CAUTION ! : It is prohibited to write "100H" to the "OAM H-position (9-bit)".
(See PPU Appendix-4)

§ 3 BG (BACKGROUND)

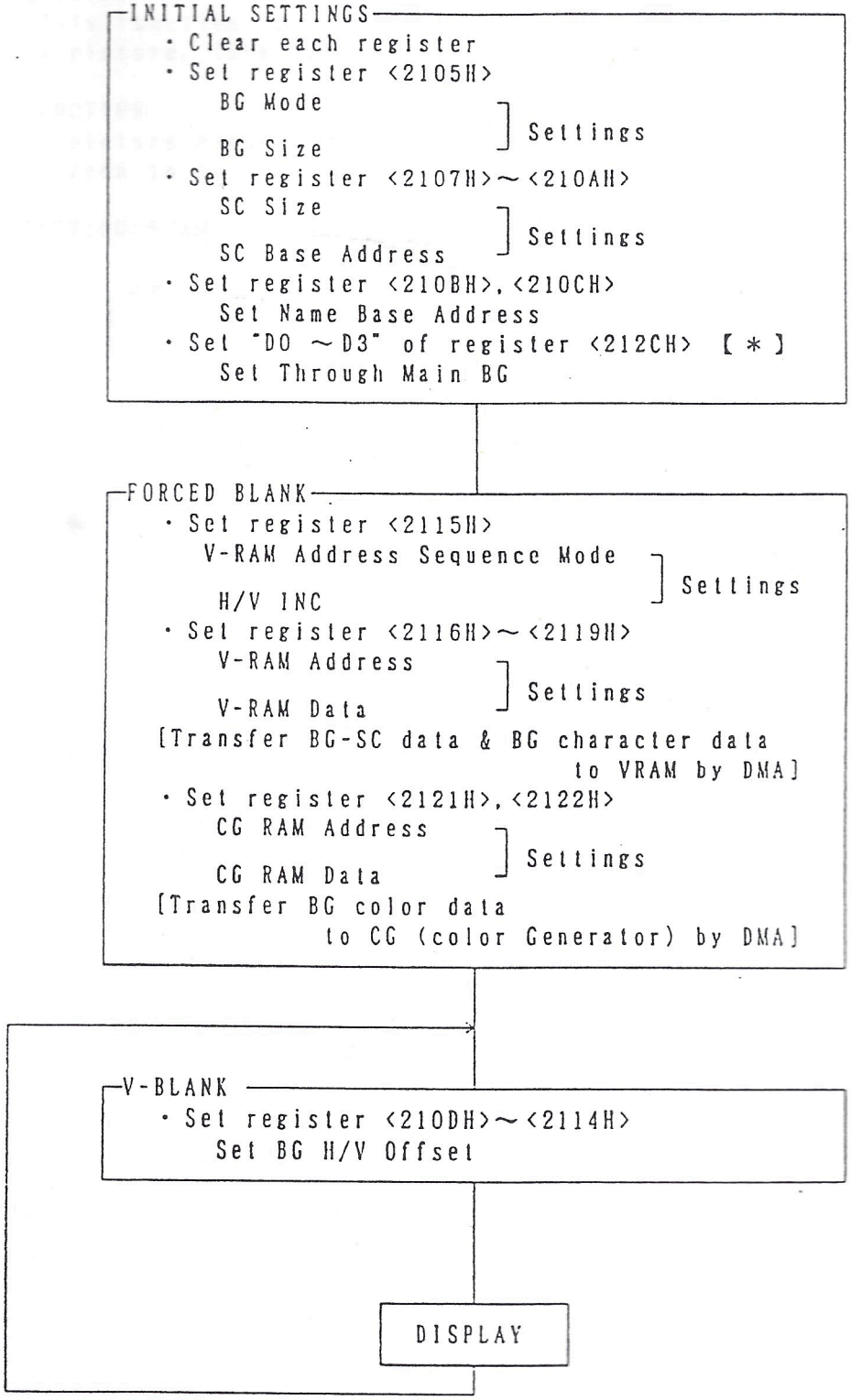
1. OUTLINE

The background for OBJ, such as Mario, can be displayed on the screen, and it can be scrolled to the up, the down, the left and the right, and it helps for the game effect.

2. FUNCTION

There are 8 kinds of BG mode.
In BG mode-0 through 6, there is a difference depending on the combination of the number of the screen, the numbers of the cell color, the resolution and the offset function.
There are 4 screens provided, and the number of the cell colors are from 4 to 256. There are 4 kinds of the resolution selected from 256-dot x 224-dot, 512-dot x 224-dot, or 512-dot x 448-dot.
The character size can be set as "8-dot x 8-dot" or "16-dot x 16-dot" on each screen.
The offset value (scroll coordinate) can be set on each BG screen, and also, the offset value can be changed every horizontal character unit depending on the mode, so that the vertical partial scroll can be made.
8 palettes can be used per character, and H-Flip or V Flip is available per character, and also, the priority order of BG and OBJ can be changed per character. (See "PPU Appendix-16")
Mode-7 has a screen, which can rotate, enlarge or reduce.
There are other functions for BG, such as the mosaic, the window, the fixed color addition/subtraction, the screen addition/subtraction, and the H-Pseudo 512.

3. SETTING EXAMPLE



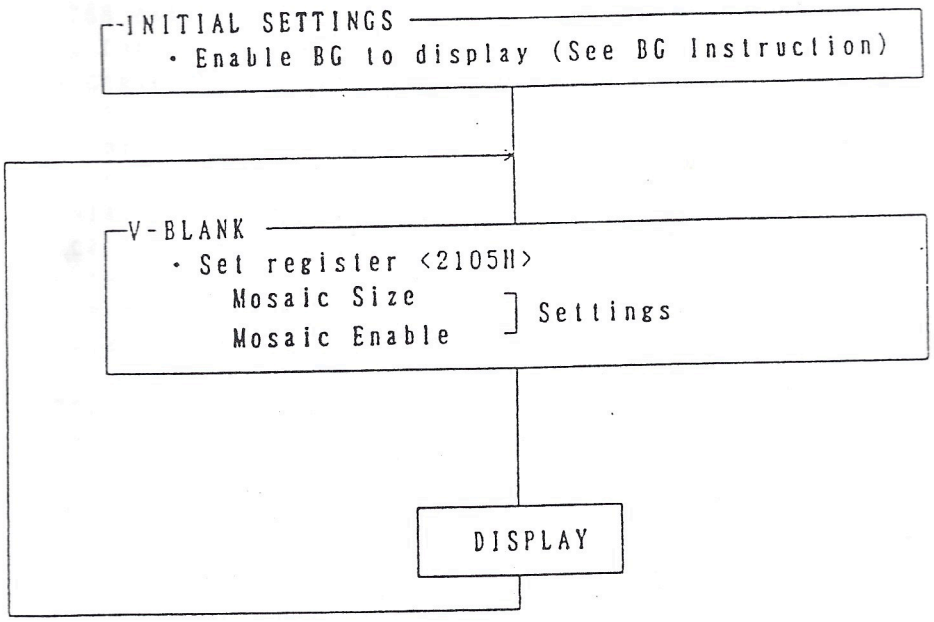
[＊] In case of BG MODE 5 or 6. "Through Sub BG" of register <212DH> should also be set. (Refer to § 7)

§ 4 MOSAIC

1. OUTLINE
   This function is to change BG screen to mosaic design and shade off a picture. (See "PPU Appendix-6")

2. FUNCTION
   A picture element of mosaic design can be changed to 15 sizes and BG screen to be a mosaic design can be selected.

3. SETTING EXAMPLE



§ 5 ROTATION/ENLARGEMENT/REDUCTION (BG MODE-7)

1. OUTLINE

In the BG mode-7, this function can add to the BG screen more animation effects by rotation, enlargement or reduction in addition to scroll function

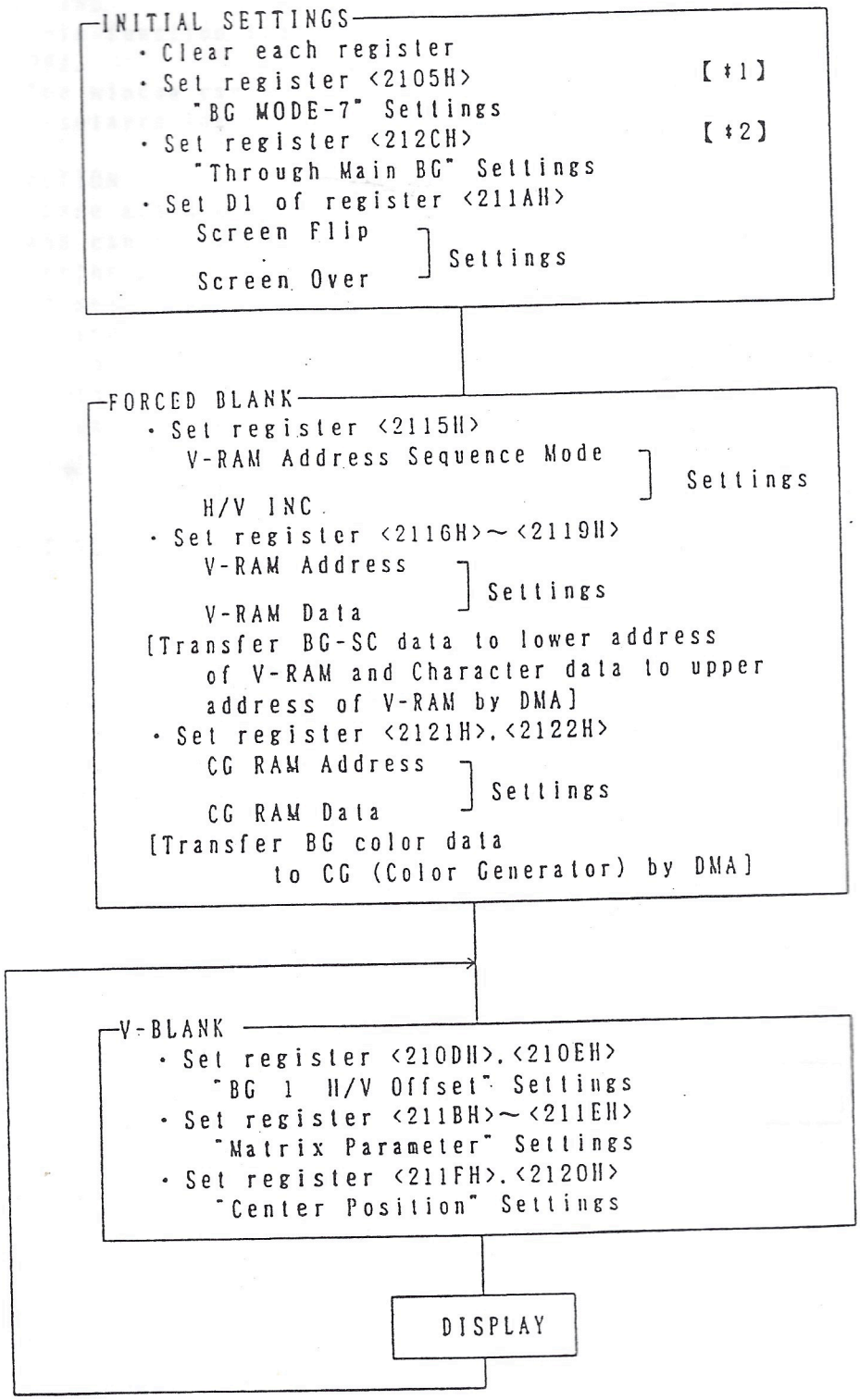
2. FUNCTION

There are 256 characters numbers (8-dot x 8-dot size).
Each dot can be one of 256 colors from a selection of 32,768 colors.
On EXTBG mode, each dot can be one of 128 colors from a selection of 32,768 colors, and each dot can have priority order.
This function is possible to scroll up, down, left and right.
The center coordinate of rotation, enlargement and reduction can be set at either outside or inside of the display area.
The rotation angle, vertical magnification, and horizontal magnification values are changeable. Also, holizontal flip and vertical flip on the display area are possible.
In case the display area goes beyond the screen area, one of three choices, which are the back drop color, a single character (CHR# 0) or repetetion (wrap) of the screen area, can be selected in order to display the excess portion.

EXTBG MODE : EXTBG mode is originally provided as a function for the purpose of the LSI BG expand.
For the SFX, it is used as rotation, enlargement and reduction with priority order.
Also, it can be used as 2nd screen on mode-7.

(See Page 61)

3. SETTING SAMPLE



[*1] On EXTBG mode, EXT. Input of register <2133H> needs to be set.
[*2] Normally, BG1 should be set. But BG2 should be set on EXTBG mode.

§ 6 WINDOW (WINDOW MASK)

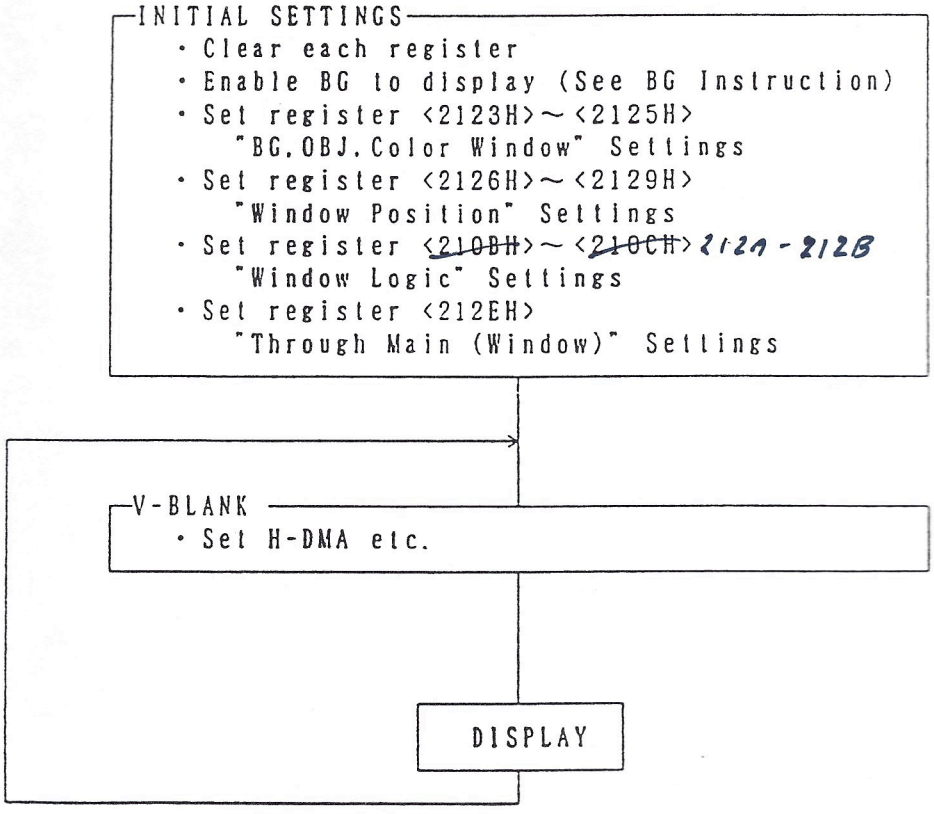
1. OUTLINE

This function limits the display area on the TV screen for BG and OBJ.
The window can be set on the TV screen, and BG and OBJ can be displayed inside (or outside) of this area

2. FUNCTION

There are 2 windows. Each window can be either BG screen or OBJ, and can be either internal or external mask.
Furthermore, 4 types of window mask logic (OR, AND XOR & NXOR) can be selected each BG and each OBJ by using 2 kinds of the windows at the same time. (See Page-57)
Moreover, if this function is combined with the function of H-DMA, various shapes of the window will be formed, such as a round shape, a heart shape or a star shape.
It is also possible to use this function combined with the screen addition/subtraction and the fixed color addition.

3. SETTING EXAMPLE



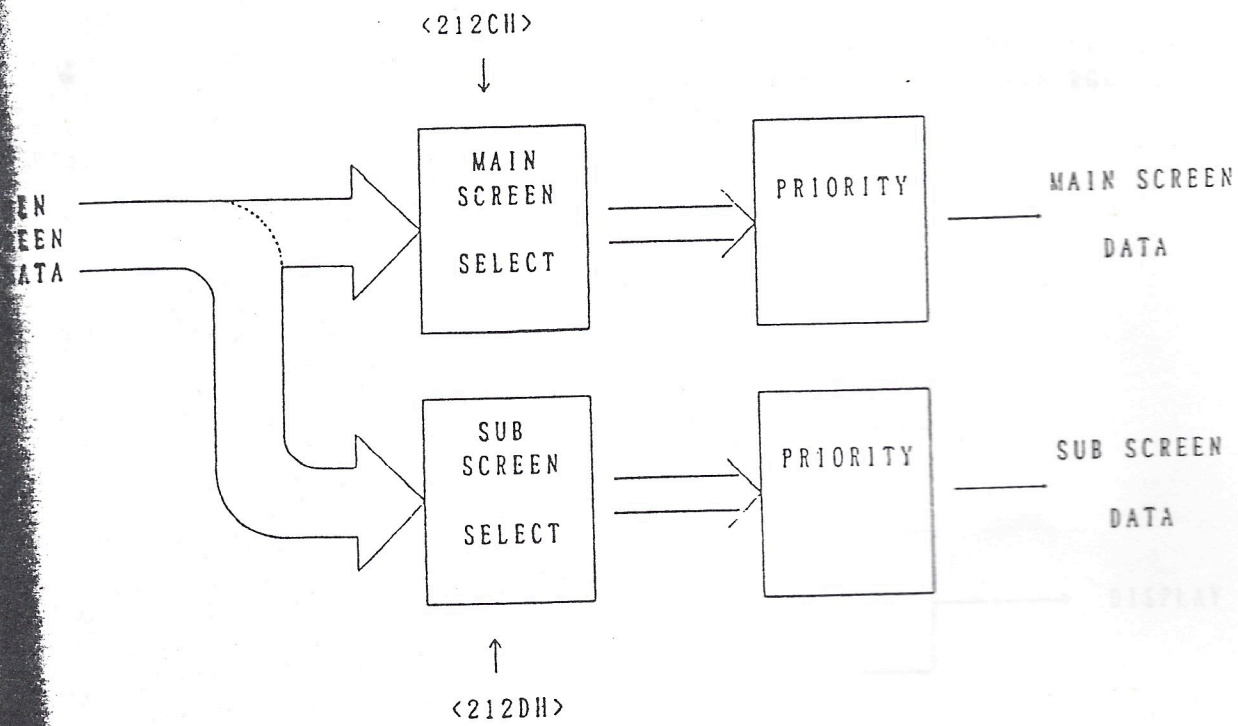
MAIN / SUB SCREEN

In case of displaying several BG and OBJ screens, the picture to be displayed in the overlapped portion is decided by two paths. One of them is called the main screen, and the other is called the sub screen.

The screen to be used for the main and the sub screen can be selected by registers <212CH> and <212DH> select.

Furthermore, the data for the main and the sub screen to be displayed is made according to the priority order.

Unless screen the addition/subtraction is done as follows, the "main sw" of the "color window" in register <2130H> is normally on, and the "sub sw" is normally off so that only the main screen is displayed. (See Appendix-20)



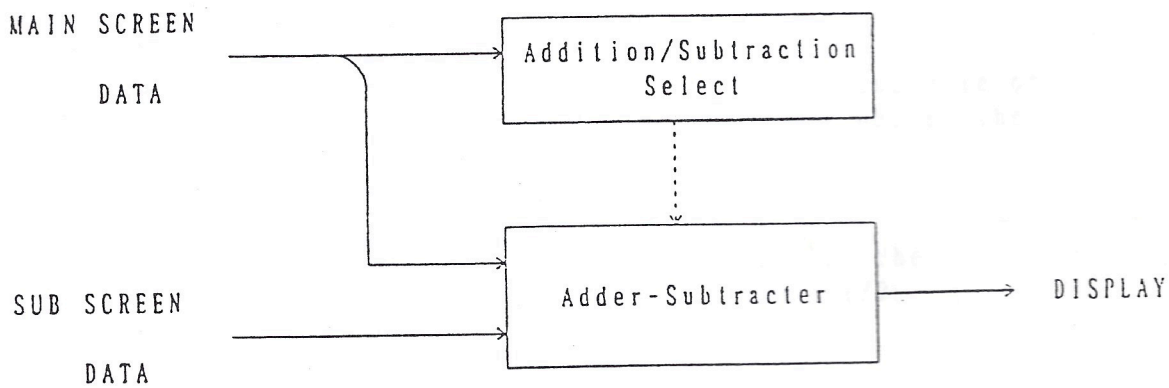
§ 7.1 SCREEN ADDITION/SUBTRACTION

1. OUTLINE

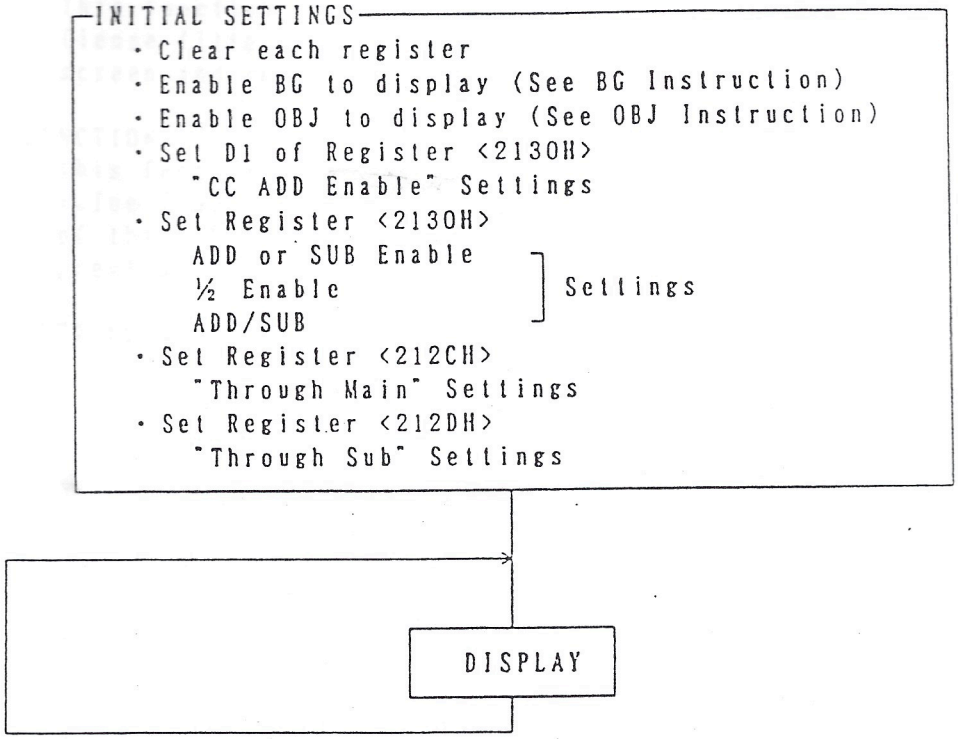
This function is the addition (Overlapping Light) or the subtraction (lense Filter) for the main screen and the sub screen in order to have the effect of transparency.

2. FUNCTION

This function indicates the result after the addition or the subtraction of RGB data on the main screen and sub screen.
This function can also select BG screen or OBJ data on the main screen to be added to or subtracted from the sub screen similar to the Fig. below.
However, when there is no screen data on the sub screen (screen is clear), the color constant explained on page 15 will be added or subtracted.
When the result added or subtracted on each RGB is over 31, the value becomes 31, also, when the value added or subtracted on each RGB is under 0, the value becomes 0.
Please do not use this function on BG mode 5 or 6.



3. SETTING EXAMPLE



NOTE : When the main screen data is the OBJ, it will be added to or subtracted from the sub screen data only for the OBJ of the palette code (4 to 7).
It is convenient for generating the dusky shadow.

NOTE : When "1/2 Enable" of register <2130H> is enabled, the addition/subtraction result of each RGB becomes 1/2.

§ 7.2 COLOR CONSTANT ADDITION/SUBTRACTION

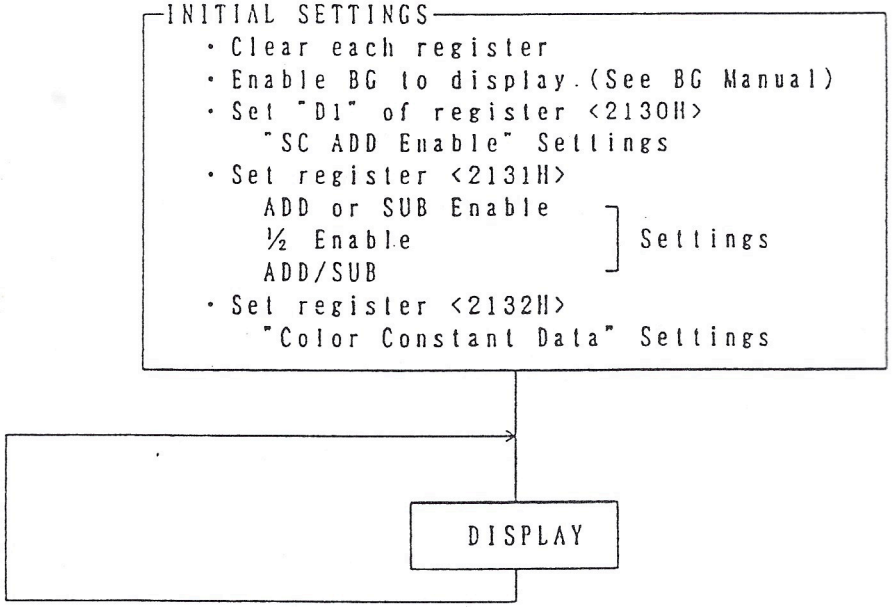
1. OUTLINE

This function can perform addition (overlapped light) or subtraction (lense filter) with the RGB value (color constant) set by the main screen and register <2132H>, and change the color on the display area.

2. FUNCTION

This function can perform addition/subtraction by using the RGB value (color constant) which is set by register <2132H> instead of the sub screen of the screen addition/subtraction described previously.

3. SETTING EXAMPLE



§ 7.3 COLOR WINDOW

(COMBINATION OF WINDOW & ADDITION/SUBTRACTION)

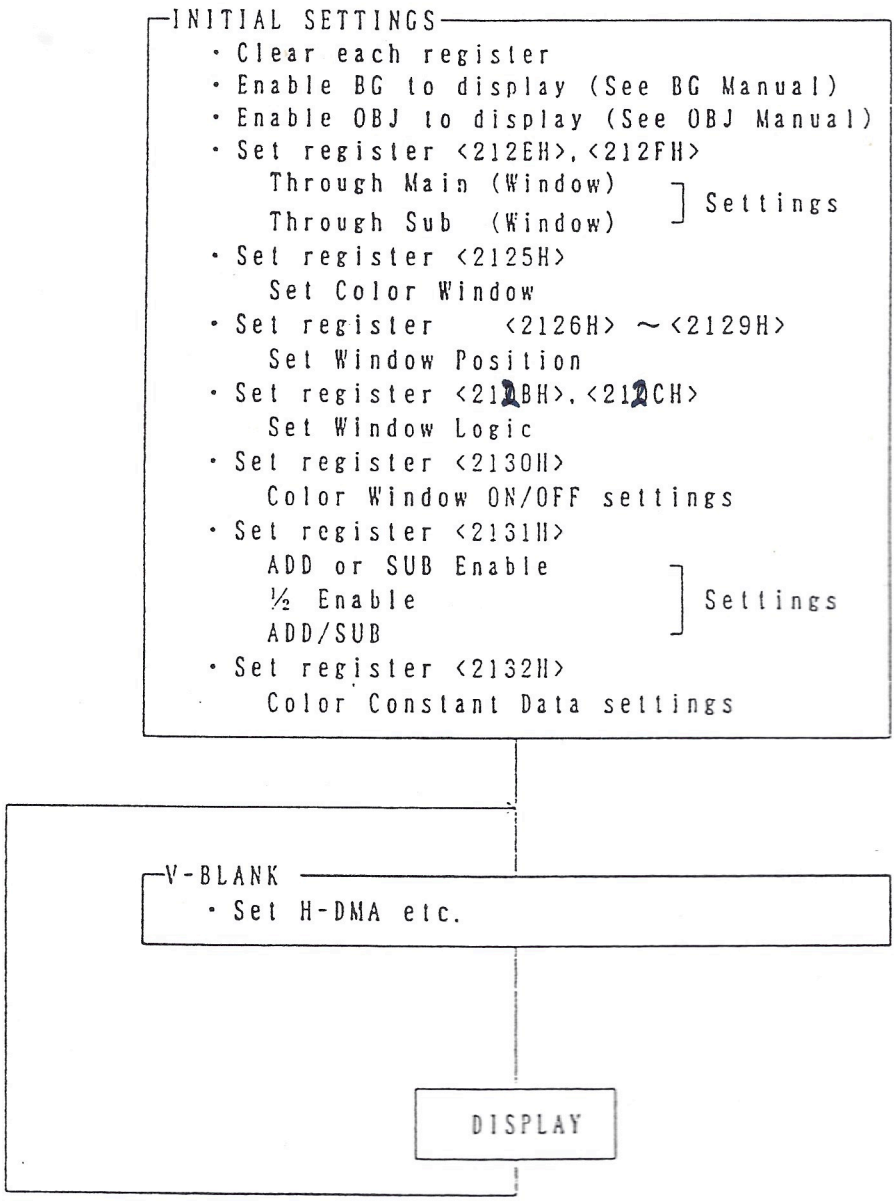
1. OUTLINE

The Screen Addition/Subtraction or the Color Constant Addition /Subtraction can be performed only inside (or outside) of the window.

2. FUNCTION

This is a function, which can select what portion of the window should be displayed and added or subtracted on each main screen and sub screen.
The following is the function as a window, the screen addition /subtraction and the color constant addition/subtraction.

3. SETTING EXAMPLE



§ 8 CG DIRECT SELECT

1. OUTLINE

On BG-1 in mode 3, 4 and 7, the character data can be used as the color data without using CG-RAM color data. BG-1 can be displayed using 2048 colors on mode 3 and 4, and 256 fixed colors on mode-7. BG-2 and OBJ can use the CG-RAM color data without holding in common with the color data on BG-1.

2. FUNCTION

When BG-1 on mode 3, 4, and 7 is displayed on the TV screen, this function is to display 8-bit color data per character dot without using the CG-RAM. the CG-RAM data is used for the other BG, OBJ and Background on main screen.

3. SETTING EXAMPLE

- Enable BG to display (See BG Instruction)
- Set "D0" of register <2130H>
  "Direct Select" Settings

NOTE : See PPU Appendix-14 for the color data.

§ 9 H-PSEUDO 512

1. OUTLINE

In the mode other than 5 and 6, this function supplements between 2 dots next to each other horizontally, which changes the color smoothly, and has the effect of the gradation.

2. FUNCTION

This function utilizes screen addition/subtraction.
The color constant addition/subtraction can not be done at the same time that this function is performed.

3. SETTING EXAMPLE

- Enable BG to display (See BG Instruction)
- Set "D3" of register <2133H>
  "Pseudo 512" settings
- Set register <212CH>, <212DH>
  Through Main
  Through Sub
  ] Settings
- Set D1 of register <2130H>
  "CC ADD Enable" settings
- Set register <2131H>
  ADD or SUB Enable
  ½ Enable
  ADD/SUB
  ] Settings

§ 1 0 COMPLEMENTARY MULTIPLICATION (SIGNED MULTIPLICATION)

1. OUTLINE

The 2's complement multiplication will be performed with high speed. For example, to calculate the rotation parameter on mode 7, it will lighten the buden of the CPU processing.

2. FUNCTION

The high speed multiplication of 16-bit (2's complement) and 8-bit (2's complement) will be performed with "no-wait", and the result becomes 24-bit (2's complement).

3. SETTING EXAMPLE

- Set BG other than MODE-7 (or V-Blank/Forced Blank)
  (except during V-Blank or Forced Blank period)
- Write lower 8-Bit (Multiplicand) to register <211BH> :(Input)
- Write higher 8-Bit (Multiplicand) to register <211BH> :(Input)
- Write register 8-Bit (Multiplier) to register <211CH> :(Input)
- Read register <2134H> ～ <2136H> :(Result)

§ 1 1 H/V COUNTER LATCH

1. OUTLINE

This function is used for judging the process timing by knowing where the scanning is approximately on the screen line at certain timing.

2. FUNCTION

This function sets vertical and horizontal counter value at certain timing (when register <2137H> is read), and know where the raster is on the screen by reading the register value.
[The Scanning synchronizes with inner vertical and horizontal counter.]

3. SETTING EXAMPLE

- Read register <2137H> : (counter latch)
- Read register <213FH>
  (Initialize register <213CH>, <213DH>
  in the order of Low and High)
- Read register <213CH>, <213DH>

§ 1 2 OFFSET CHANGE

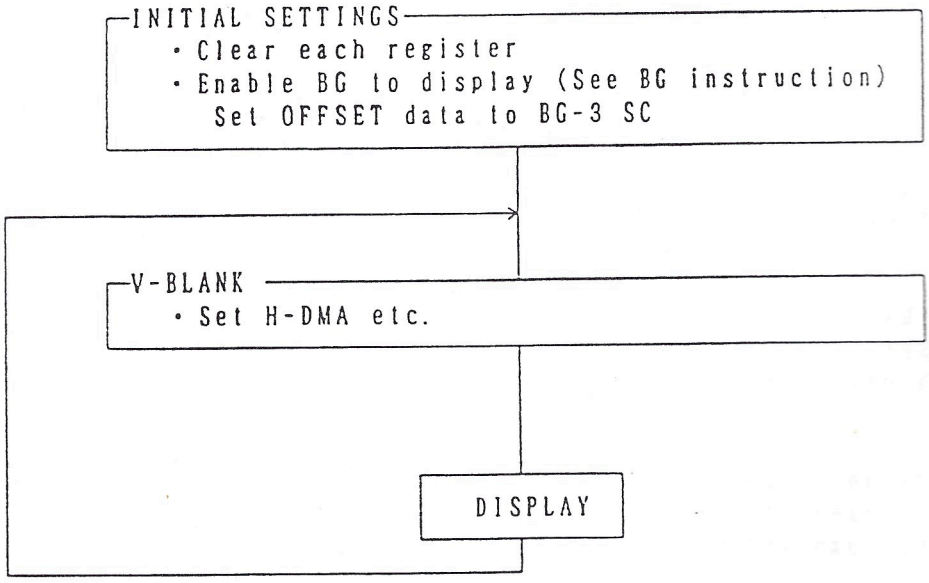
1. OUTLINE

The horizontal and vertical scroll (offset) value can be performed every horizontal 8-dot (character unit) in mode 2, 4 and 6.
The other part of the screen can be brought in the middle of the frame in order to have the effect like a window, and also, a vertical partial scroll can be made.

2. FUNCTION

This function can be selected whether both BG-1 and 2, or either BG-1 or 2 are applicable. The offset for both H and V can be changed at every character unit on mode-2 and 6, but the offset for either H or V can be changed on mode-4.
The same offset will be performed on each line, once the offset data for a horizontal line (32-characters) is set.
In case of setting the other offset value depending on the scanning line, the offset can be changed by changing "BG-3 SC Offset Address" or "BG-3 SC Base Address" during the H-DMA period.

3. SETTING EXAMPLE



§ 1 3 JOY CONTROLLER

1. OUTLINE

The switch status of the joy controller can be read automatically serially, and it will be converted to the parallel data.
It is not necessary to read the switch status one by one like the Family Computer and convert them to the parallel data every time.

2. FUNCTION

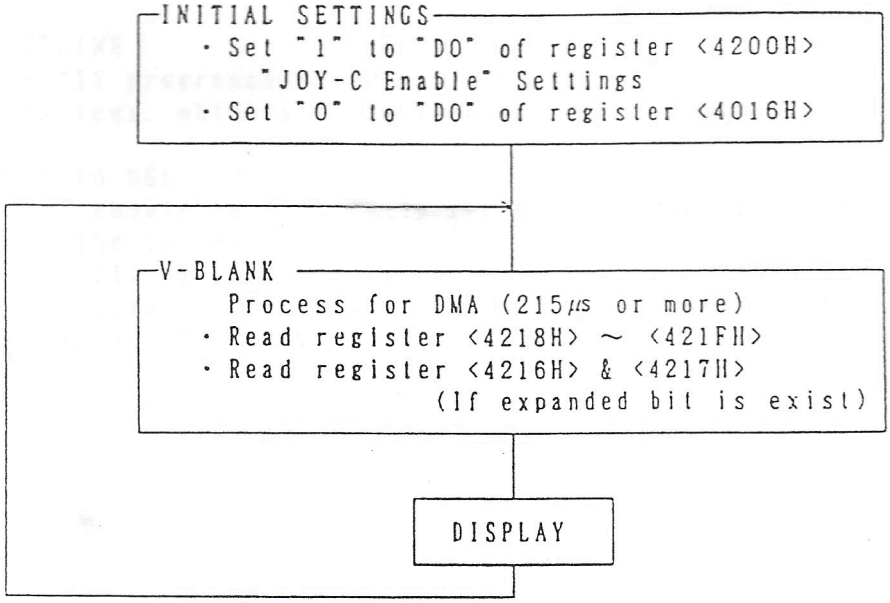
2 pcs of the Joy controller can be connected to the main unit.
(4 pcs of the Joy controller can be connected by using the expanded connector.)
1-bit data is assigned to each switch, and the number of bits to be read automatically for one Joy Controller is up to 16-bit.
For the expanded bit, the bit which is expanded can be read 1-bit by 1-bit by the software like the Family Computer.
The hardware operates for reading the data for about 215 μs right after the V-Blank flag is set or the NMI is applied. Therefore, please note that the register of the Joy Controller can not be read properly.

☆ 215 (214.55)μs is equivalent to 3.4 (3.38) scanning lines, which is a period of 580 (576) Byte to be transfered by the DMA. (In case the CPU clock is 2.68MHz, it is equivalent to 580 machine cycle.)
as soon as the V-Blank starts,
it is considered as the basic flow to perform the general purpose DMA.
Therefore, It is convenient if total number of byte to be transfered by the general purpose DMA is used as a read timing.
[Please refer to the System Flowchart]

☆ The Joy Controller data (register) should be read after confirming that "JOY-C Enable" of the register <4212H> is not set during the V-Blank period, so that the valid data can be read.

* After 18μs (32 machine cycle with 2.68MHz) from the beginning of the V-Blank, the hardware will start to read.
The "JOY-C Enable" of the register <4212H> can not be set during this period.

3. SETTING EXAMPLE



§ 1 4 PROGRAMABLE I/O PORT

1. OUTLINE

   8-BIT programable I/O port is provided to interface to peripheral devices. which are the keyboard, the 3D-glass and etc.

2. HOW TO USE

   "1" should be written to register <4200H> for the bit to be used as the in-port.
   The bit becomes the In-port and it can be read by register <4213H>.
   The data should be written to register <4201H> for the bit to be used as the Out-port.
   This written data can be output directly.

§ 1 5 ABSOLUTE MULTIPLICATION/DIVIDE

1. OUTLINE

The absolute multiplication (8-bit x 8-bit) and the absolute divide . (16-bit x 8-bit) can be done using this function.
It is also convenient for the array table processing, and it can improve the processing speed for the multiplication and the divide.

2. FUNCTION

The multiplication calculation between the multiplicand of 8-bit absolute value (0～255) and the multiplication of 8-bit absolute value (0 ～255) can be performed, and can get the result of 16-bit product (0 ～65025).
Or, the divide calculation between the dividend of 16-bit absolute value (0 ～65535) and the divisor of 8-bit absolute value (0 ～255) can be performed, and can get the result of 16-bit quotient (0 ～65535) and 16-bit remainder.
If the divisor is "0" in the divide calculation, the quotient value becomes 65535 (0FFFFH) and the remainder becomes the dividend value, so that caution is required.
It takes about 8 machine cycle for the multiplication calculation and about 16 machine cycle for the divide calculation.
The register value for multiplicand and dividend will not be destroyed even after operation.

3. SETTING EXAMPLE

```
*  In case of Multiplication :
       · Set register <4202H>
           "Multiplicand-A" Settings
       · Set register <4203H>
           "Multiplier-B" Settings
       · Wait for 8 Machine Cycle
       · Read register <4216H>,<4217H>
           Read Product-C

*  In case of Divide :
       · Set register <4204H>,<4205H>
           "Dividend-C" Settings
       · Set register <4206H>
           "Divisor-B" Settings
       · Wait for 16 Machine Cycle
       · Read register <4214H>,<4215H>
           Read Quotient-C
       · Read register <4216H>,<4217H>
           Read Remainder
```

§ 1 6 H/V COUNT TIMER

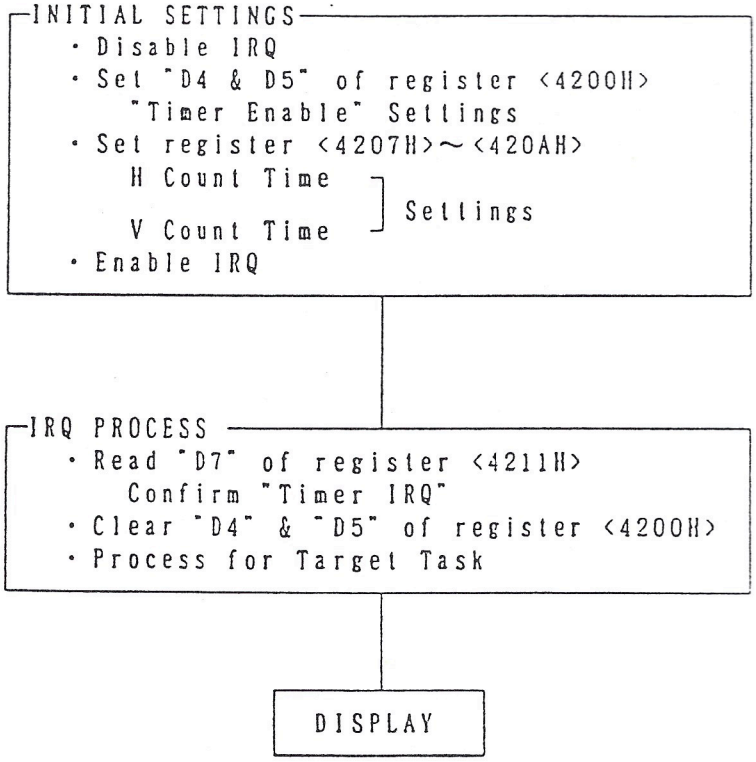
1. OUTLINE

The SFX has the timer synchronizing with the display on the TV screen, which is used for adjusting the timing of the scanning on the screen and the software process.

2. FUNCTION

This function can generate the interrupt either at any V-position or H-position of the scanning lines. It can also generate the interrupt at any position of the scanning line.

3. SETTING EXAMPLE



§ 1 7 DMA (DIRECT MEMORY ACCESS)

The DMA is the method to transfer the data as same as the data transfer which is done by the CPU. However, the DMA can transfer the data at high speed by using the hardware instead of the CPU.
Especially, the SFX has the exclusive DMA, since the picture data has to be transfered rapidly.
The DMA for the SFX is to transfer the data between "A-Bus address" in the CPU (0000000～0FFFFFF) and "B-Bus address" in the S-PPU (0002100 ～00021FF), which has 8-channels in total.
There are two kinds of the DMA, which are the general purpose DMA and the H-DMA, and either of the two can be set at each channel.
The data can be transfered between the same DMAs in the order from the lower channel number (0 ～7). And the H-DMA can interrupt even during the transfer by the general purpose DMA, which means that the H-DMA has higher priority than the general purpose DMA.
Furthermore, the CPU process stops automatically during the DMA period, and will start again after the DMA is completed. Therefore, it is not necessary to observe the DMA completion by the CPU.

§ 17.1 GENERAL PURPOSE DMA

1. OUTLINE

This function can transfer the data rapidly between 2 types of memory devices, which is memory which can be accessed directly by the CPU, such as a ROM on the game cartridge, and memory which has to be accessed through the S-PPU, such as the V-RAM.

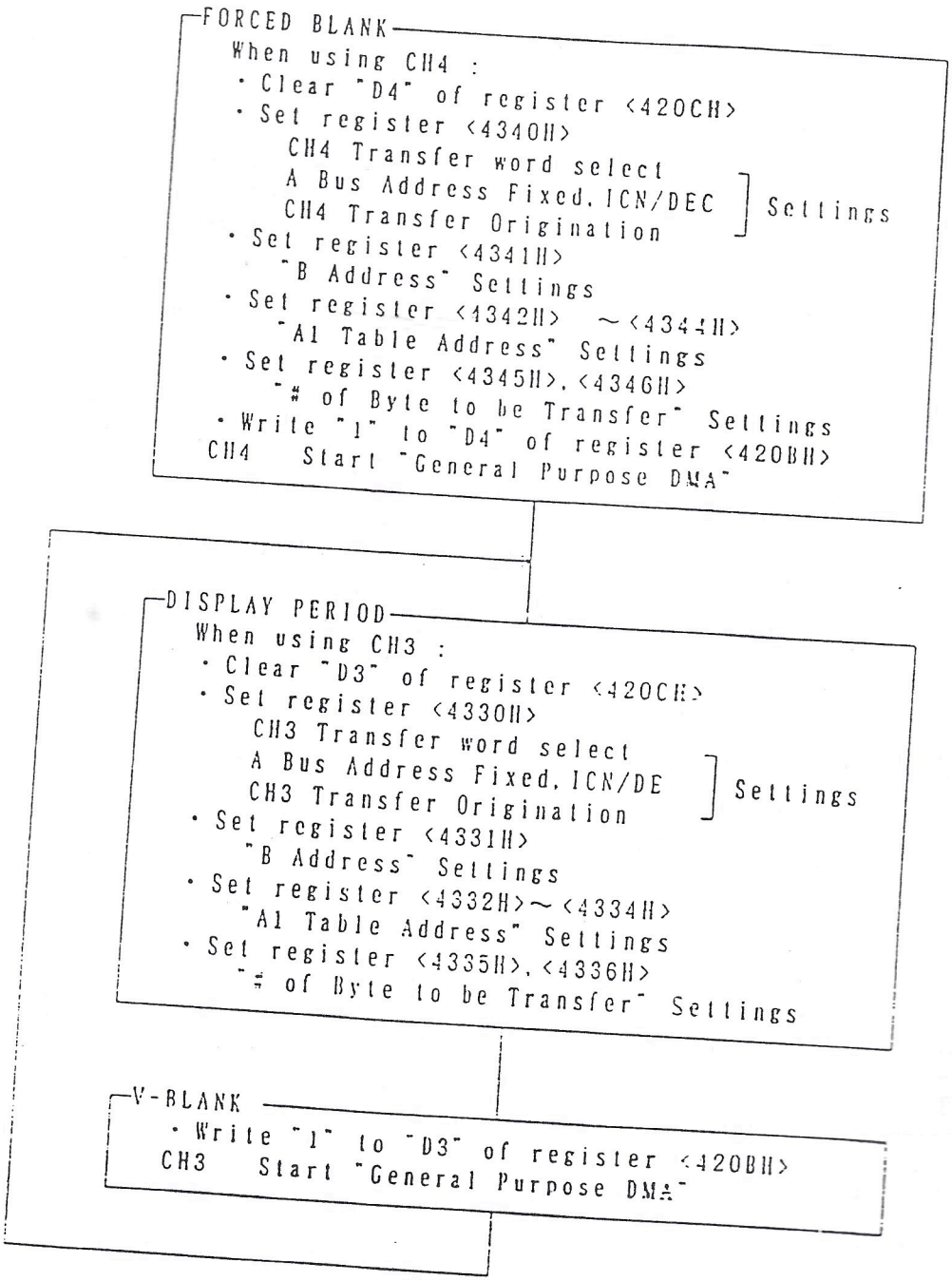
2. FUNCTION

The maximum area of the A-Bus address which can be used in one channel is limited in one bank (65,536 Byte).
Therefore, in case of spreading over more than 2 banks, it is necessary to use more than 2 channels or transfer twice.
One A-Bus address basically is increased every time 1-byte data is transfered. However, it can be decreased or fixed depending on the settings ("D3" and "D4" of register <43X0H>).
The following table shows 4 ways of the B-Bus address changes.

Transfer Word Select <43X0H> / # of Transfer (# of Byte)	0 or 2	1	3	4
0	B	B	B	B
1	B	B + 1	B	B + 1
2	B	B	B + 1	B + 2
3	B	B + 1	B + 1	B + 3
4	B	B	B	B
5 . . .	B . . .	B + 1 . . .	B . . .	B + 1 . . .

NOTE : B means the data of register <43X1H>.

☆ In case of 224-lines, the general purpose DMA can transfer 6K-Byte data maximum during V-BLANK period.


FORCED BLANK
When using CH4 :
· Clear "D4" of register <420CH>
· Set register <4340H>
CH4 Transfer word select
A Bus Address Fixed, ICN/DEC
CH4 Transfer Origination
Settings
· Set register <4341H>
"B Address" Settings
· Set register <4342H> ~ <4344H>
"A1 Table Address" Settings
· Set register <4345H>, <4346H>
"# of Byte to be Transfer" Settings
· Write "1" to "D4" of register <420BH>
CH4 Start "General Purpose DMA"
DISPLAY PERIOD
When using CH3 :
· Clear "D3" of register <420CH>
· Set register <4330H>
CH3 Transfer word select
A Bus Address Fixed, ICN/DE
CH3 Transfer Origination
Settings
· Set register <4331H>
"B Address" Settings
· Set register <4332H> ~ <4334H>
"A1 Table Address" Settings
· Set register <4335H>, <4336H>
"# of Byte to be Transfer" Settings
V-BLANK
· Write "1" to "D3" of register <420BH>
CH3 Start "General Purpose DMA"

§ 17.2 H-DMA

1. OUTLINE

This is the special DMA, which can transfer the data automatically synchronizing with the H-Blank. Therefore, the S-PPU settings can be varied by each horizontal scanning line, and also, special effects can be added to the picture.

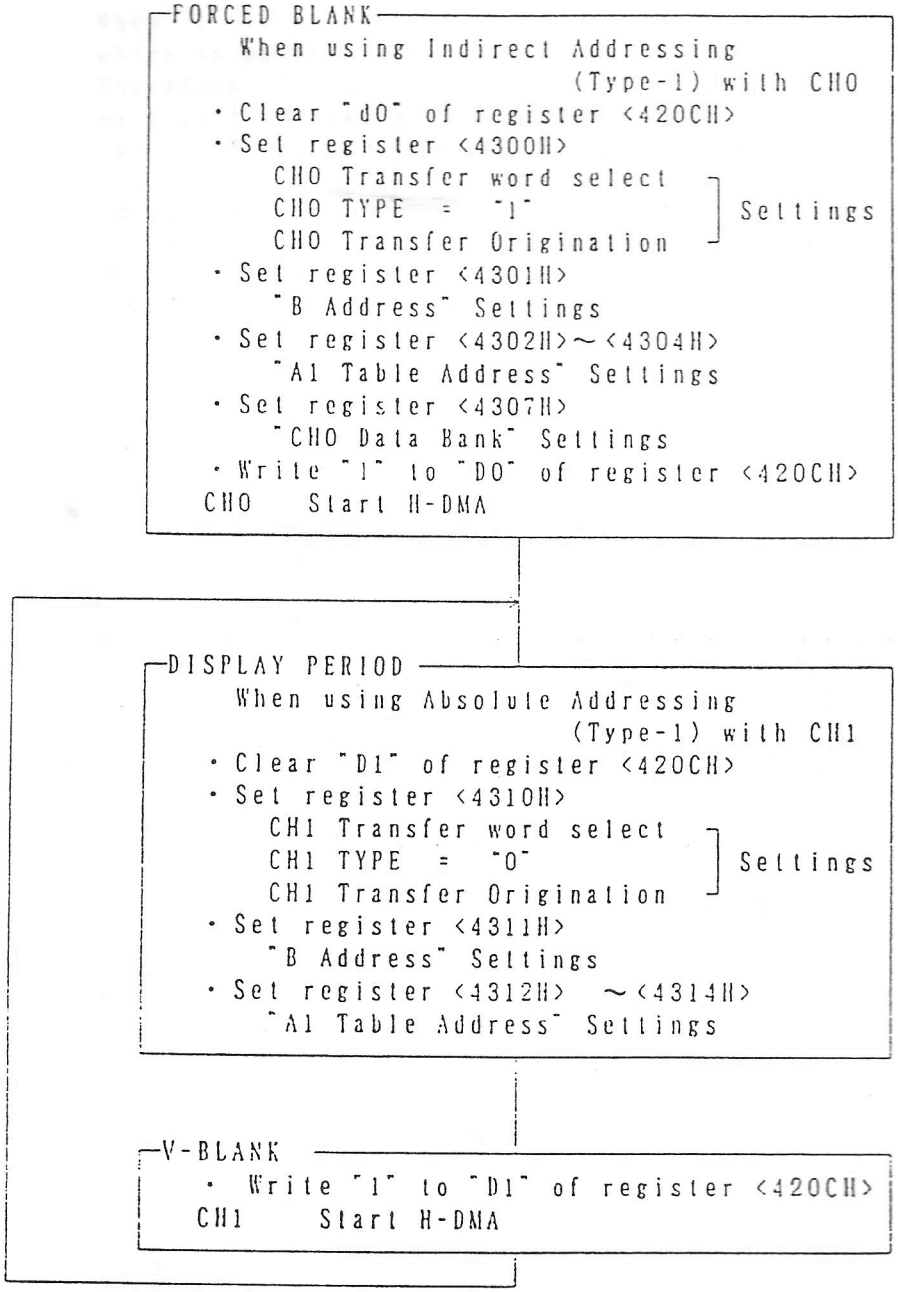
2. FUNCTION

This function basically transfers the data from the A-Bus memory (CPU memory) to the S-PPU register.
There are two kinds of the addressing modes on the A-Bus side, absolute addressing and indirect addressing, which can be set by each channel.
There are two kinds of the data transfer, one is to transfer a set of data each horizontal blank period, and the other is to transfer a set of data every certain number of the horizontal blanks.
These two methods can both be used in the data table for one screen (one field), therefore, necessary data can be transfered each necessary scanning line for one screen (one field).
The B-Bus address can be changed five ways according to the table shown below.

# of Line to be Transfered \ Transfer word select <43X0H>	0	1	2	3	4
1	B	B	B	B	B
				B	B + 1
		B + 1	B	B + 1	B + 2
				B + 1	B + 3
2	B	B	B	B	B
				B	B + 1
		B + 1	B	B + 1	B + 2
				B + 1	B + 3
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.

NOTE : B means the data of register <43X1H>.

3. SETTING EXAMPLE



S 1 8 INTERLACE

1. BG MODE 0 ~ 4 & 7

   When "1" is written to "D0" of register <2133H>, the picture which is output from the SFX will be the interlace signal. Therefore, in case of BG mode 0 through 4 and 7, the same picture will be displayed unless the picture data is changed between the 1st field and the 2nd field. (See PPU Appendix-18)

2. BG MODE 5 & 6

   In case of the interlace on BG mode 5 and 6, the vertical resolution will be doubled in appearance, because a picture is displayed by using one frame of the combination of the 1st field and the 2nd field. (See Appendix-19)

3. OBJ

   When "1" is written to "D1" of register <2133H>, the vertical resolution will be doubled as same as the case above, because a picture is generated by one frame.
   However, the range of the V-position is 0 through 255, and it will not be doubled.

§ 1 9 H- 512 MODE (BG MODE 5 & 6)

1. MAIN SCREEN & SUB SCREEN SETTINGS

   The screen addition/subtraction should not be used, because a part of both main screen and sub screen function are used in this mode. Therefore, for the case except the color constant addition /subtraction, "1" should be written to "D4" and "D5" of register <2130H> and the sub switch should be "OFF".
   Also, in this mode, the same data should be written to registers <212DH> <212EH> and <212FH>, and "Through" should be the same for both the main and the sub screen.

2. FIXED COLOR ADDITION/SUBTRACTION

   "D0 ~ D5" of the register <2131H> is the flag which can select the main screen for addition/subtraction.
   By the reason described above, this selection can not be done.
   It is necessary to write "1" to these 6 flags (D0 ~ D5) when the color constant addition/subtraction is performed.
   The remaining settings are the same as the other mode on page 15.
   However, in case of the color window function, there will be addition/subtraction every 2-dot unit horizontally, because the window has only 256 positions horizontally.

3. DISPLAY WITH OBJ

   As the name of H-512 mode implies , it indicates the 512 horizontal resolution for BG. But, the horizontal resolution for the OBJ is only 256-dot regardless of the BG mode.
   However, the priority order for BG is determined by every dot.

4. OTHERS

   See Appendix-19 for details

§ 2 0 OBJ 33'S LINES OVER & PRIORITY ORDER

1. 33's RANGE OVER

The number of OBJ which can be displayed in a horizontal line is limited. One of its limitation is called the "33's Range Over". This is the limitation that OBJs (33 or more) can not be displayed in a horizontal line regardless of the OBJ size.
If the "33's Range Over" is occured in one field (at least one line), "D6" of the register will be set.
For the line which this "33's Range Over" is occured, only 32 OBJs can be displayed out of more than 33 OBJs according to the priority order (selected from smaller OBJ number).

NOTE : "the number of displayed OBJ" counts the OBJ hidden by BG, window or other OBJs.

NOTE : If H-position is minus, and the OBJ is not displayed on the screen area to be displayed (located on the left of the left the screen to be displayed), "the number of the displayed OBJ" does not count them.

2. 35's TIME OVER

The other limitation on one horizontal line is the "35's time over". This is the limitation that OBJ character size is converted to character size (8-dot x 8-dot) and OBJs (35 or more) can not be displayed
If the "35's Time Over" has occured in one field (at least one line), "D7" of the register <213EH> will be set.
In the line which this "35's Time Over" has occured, only 32 OBJs out of "The OBJ which should be displayed" can be displayed according to the priority order (selected from larger OBJ number).
The other limitation on one horizontal line is the "35 time over". This limit is due to a conversion limit of less than 35 OBJs (8 x 8) displayed per horizontal line.
"The OBJ which should be displayed" means less than 33 OBJs which satisfy the display condition explained in "33's Range Over" above.

NOTE : There are characters (8-dot x 8-dot) which are not displayed on the display area depending on OBJ size and position. But they are not included in this limitation (34 or less).

3. PRIORITY ORDER SHIFTING

As mentioned above, limited numbers of the OBJs can be displayed in a line and are related to the priority order. It is desirable to develop a game within this limitation. However, more OBJs beyond this limitation sometimes need to be displayed. In this case, there is the way to display more OBJs imaginarily on one line. The priority order which is changed every frame is one of the methods. Also, there is another method, which changes the OBJ data order by programming. The SFX also has the function to rotate the priority order of 128 OBJs.
When using these methods, please consider that the OBJ will flash every frame unit, and the priority order among OBJs will change.
The setting method is as follows:

① display the OBJ.
② Write "1" to "D7" of the register <2103H>.
③ Write the highest priority OBJ number (0 ～ 127) to "D1～D7" of the register <2102H> during V-BLANK period every frame.
④ repeat ③

When OBJ number storing at ③ is "n"

OBJ NUMBER	PRIORITY ORDER
OBJ 0	129－n
・ ・ ・	・ ・ ・
OBJ n－1	128
OBJ n	1
OBJ n＋1	2
・ ・ ・	・ ・ ・
OBJ127	128－n

§ 2 1 CPU CLOCK & ADDRESS MAP

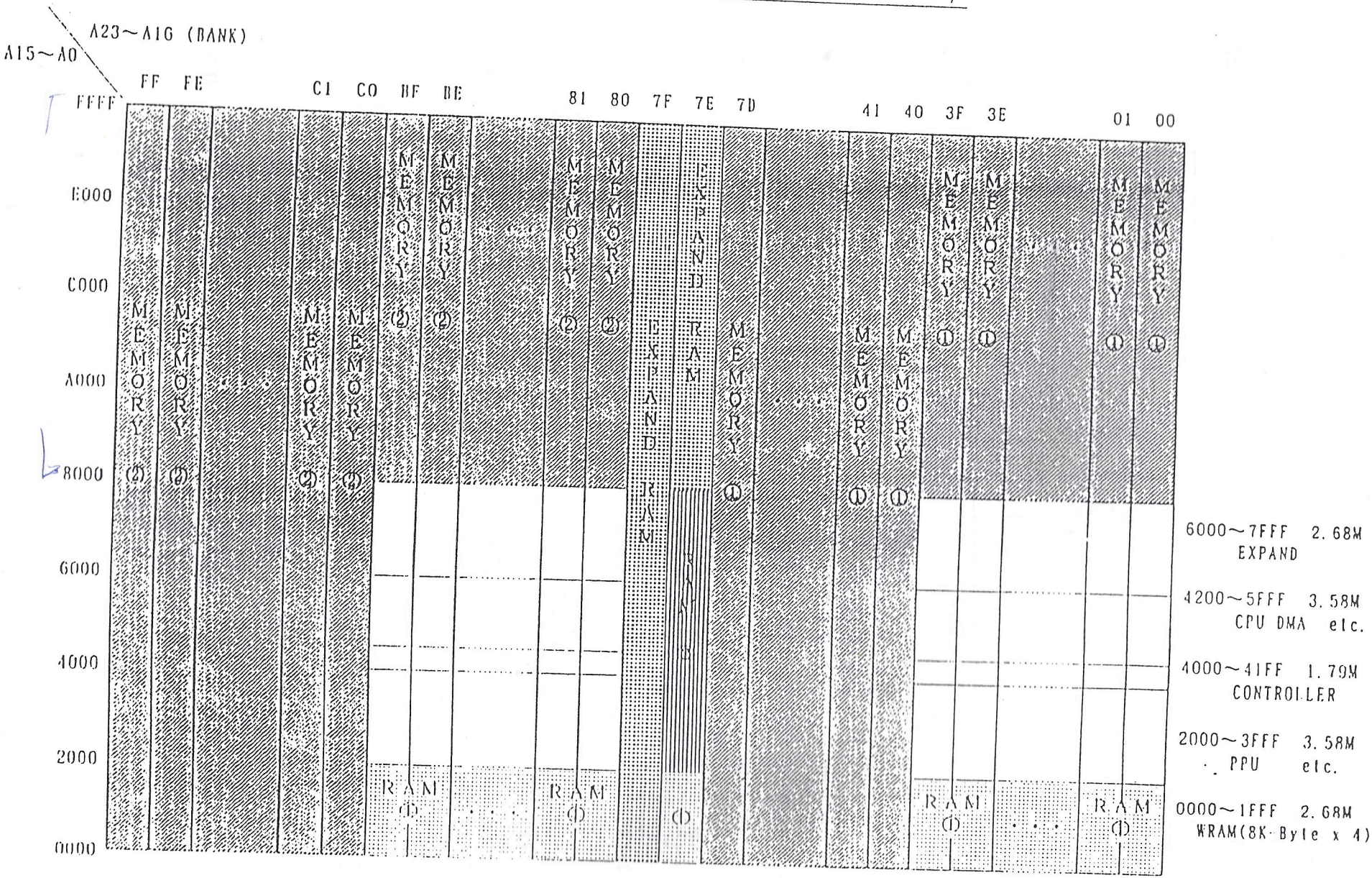
1. CPU CLOCK

The CPU clock can be switched automatically depending on the address to be accessed by the CPU.
There are 3 kinds of clock speed, which are 3.58MHz, 2.68MHz, 1.79MHz, and they can be used according to the device speed (ROM, RAM, LSI and etc.).
If the ROM and RAM of middle speed (access time less than 200ns) are used in the cartridge, it will be mapped to the address area (2.68MHz). If high speed (access time less than 120ns) are used, it will be mapped to the address area (3.58MHz).
[At present (as of January, 1989), because most of the ROM and the RAM used in the video games are designed for more than 150ns speed, 2.68MHz clock is used as the standard.]
Please refer to the "Frequency & Address Mapping" for the relation between the address and the clock.
Two clocks (2.68MHz & 3.58MHz) can be selected by setting "D0" of register <420DH> for the range of memory ② shown on illustration. And 2.68MHz is set as default.
The CPU is operated internally with 3.58MHz clock speed.
[Regardless of the address, the DMA will be operated with 2.68MHz clock speed.]

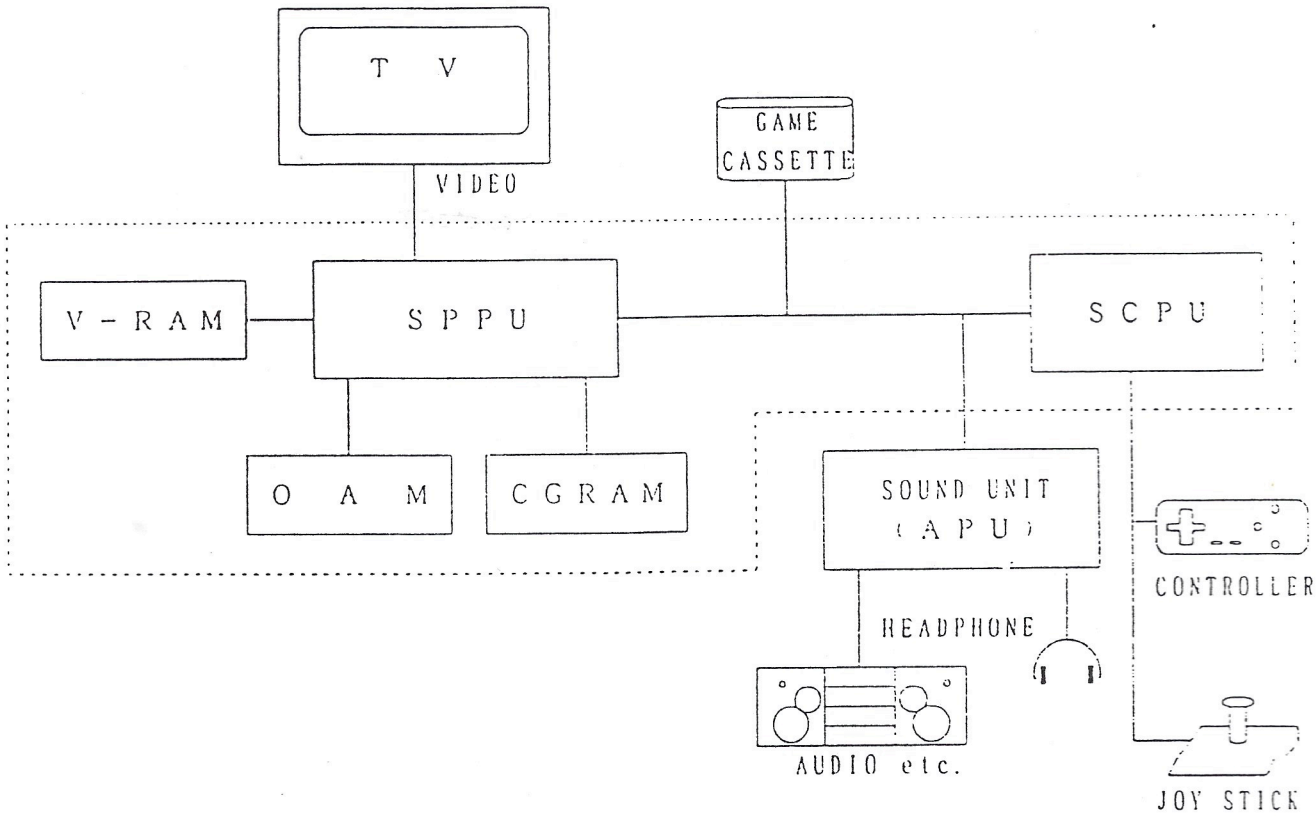
2. ADDRESS MAP

Please refer to the "Frequency & Address Mapping".
The WRAM (8K-Byte) is mapped to the address (0000～1FFF) of the bank (00 ～3F), (80 ～BF) and 7E.
Because this is the WRAM used as common bank, this 8K-Byte can be accessed from any bank described above.
Also, the WRAM (24K-Byte) is mapped to the address (2000 ～ 7FFF) of the bank 7E. Therefore, the WRAM (32K-Byte in total) is included in the SFX unit. The address (8000 ～ FFFF) of the bank 7E and the address (0000～ FFFF) of the bank 7F are provided as extra area for expanded WRAM.
Also, the address "2000～ 5FFF" of the bank "00～3F" and "80 ～ BF" are reserved as a register area of the S-PPU, DMA, etc.
Also, because this basically is reserved as a common bank area, the S-PPU and the DMA register can be accessed from any bank.

CPU SYSTEM CLOCK (FREQUENCY & ADDRESS MAP)



§ 2 2 HARDWARE CONFIGURATION



§ 22.1 NAME & FUNCTION

SCPU (CPU) · · · · · · This is a Central Processing Unit for the SFX.
This is equivalent to the SFX's brains. forwards the game according to the program data in cassette and has the useful function for the game.

SPPU (PPU) · · · · · · This is a Picture Processing Unit for SFX.
This is equivalent to the SFX's hands or legs. which generates various pictures according to the control from the CPU and has the function to vary image expression.

SOUND UNIT (APU) This is a Audio Processing Unit.
This is equivalent to the SFX's mouth. which generates produces necessary music or sound effect for the game and has the functien to vary sound expression.

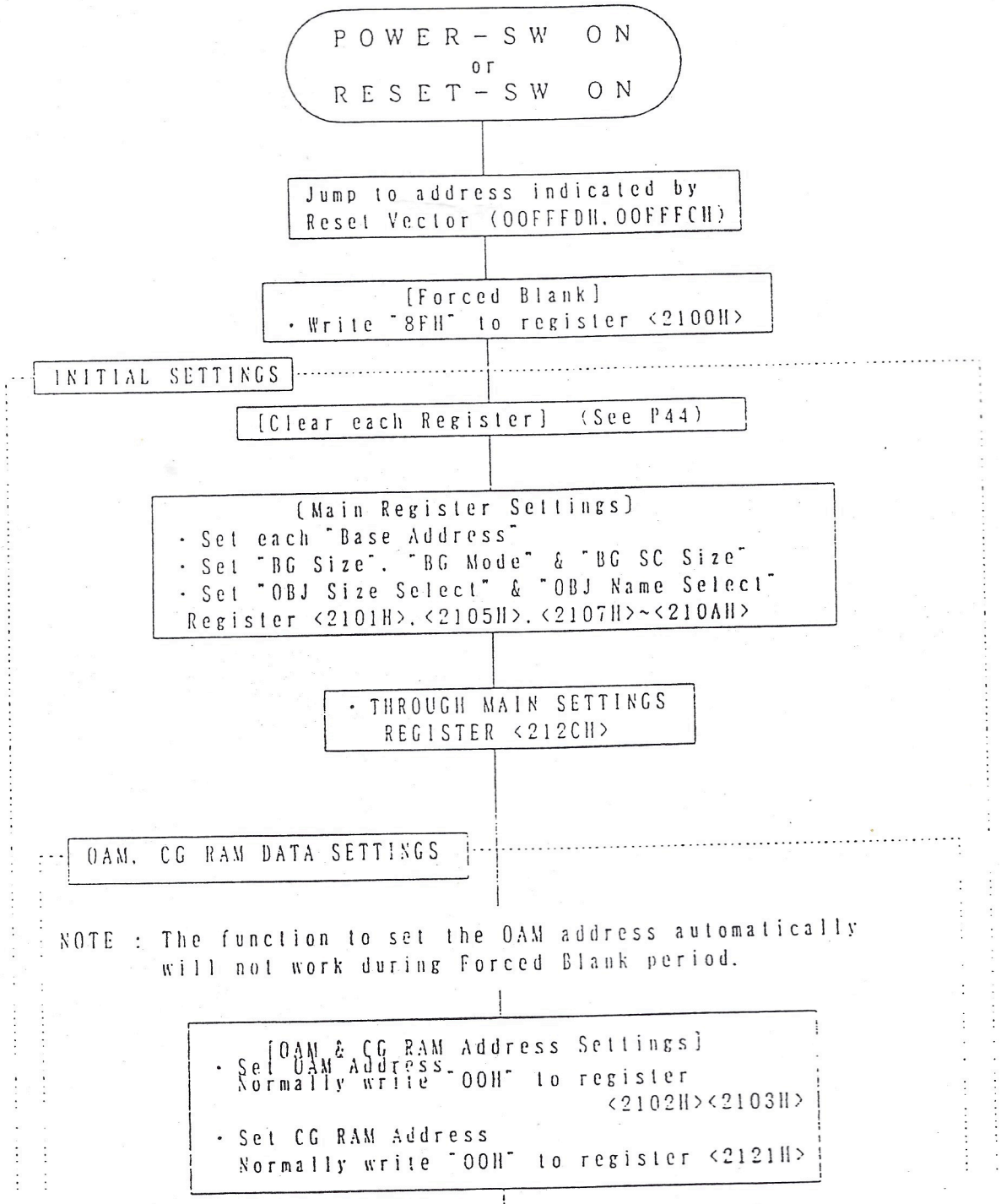
GAME CASSETTE・・ This is the memory to store necessary data, which is program data, character data or sound data.

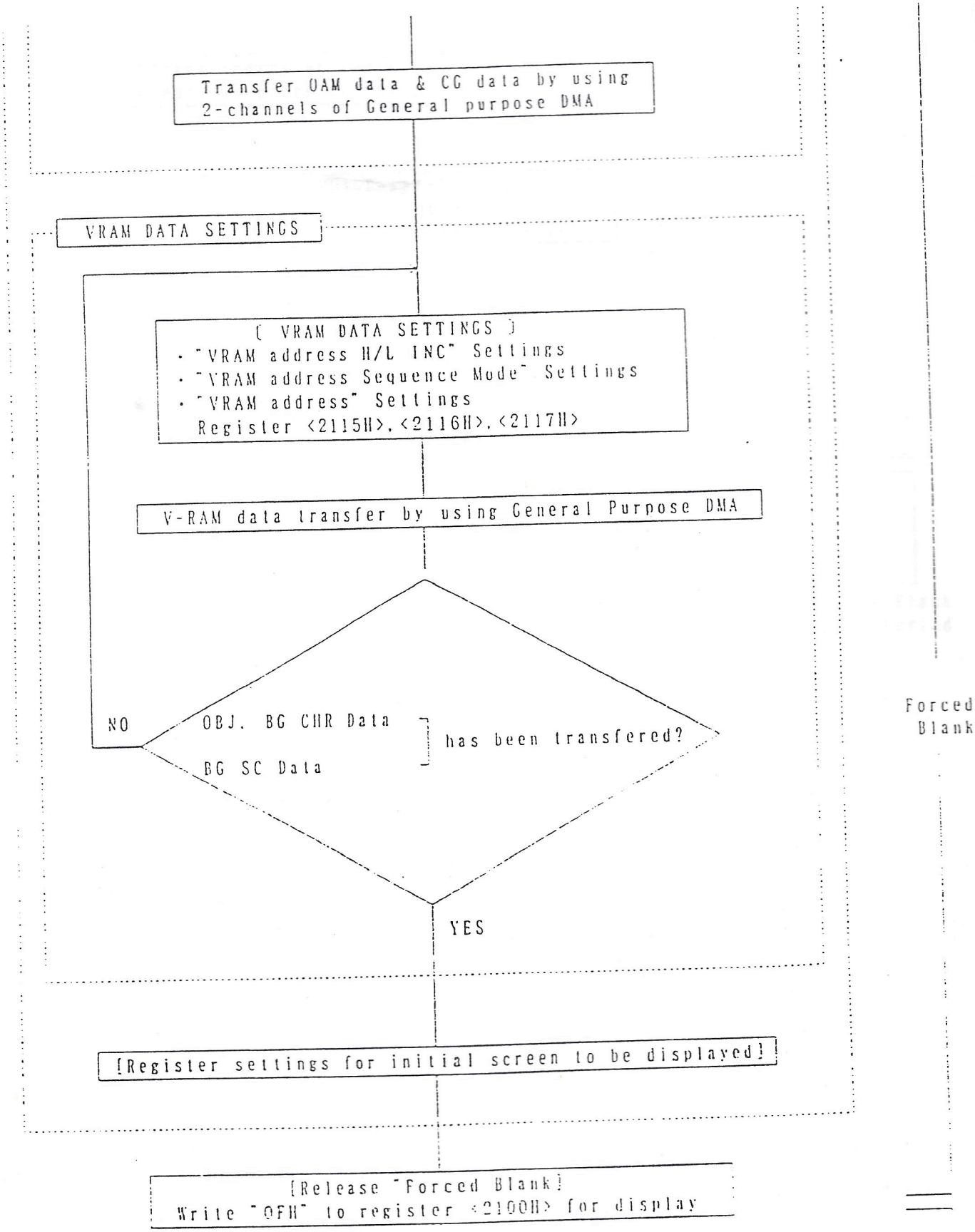
OAM・・・・・・・・・・・・ This is a Object Attribute Memory (OAM). This is used to store necessary data to move characters, such as the hero or enemy in the game.

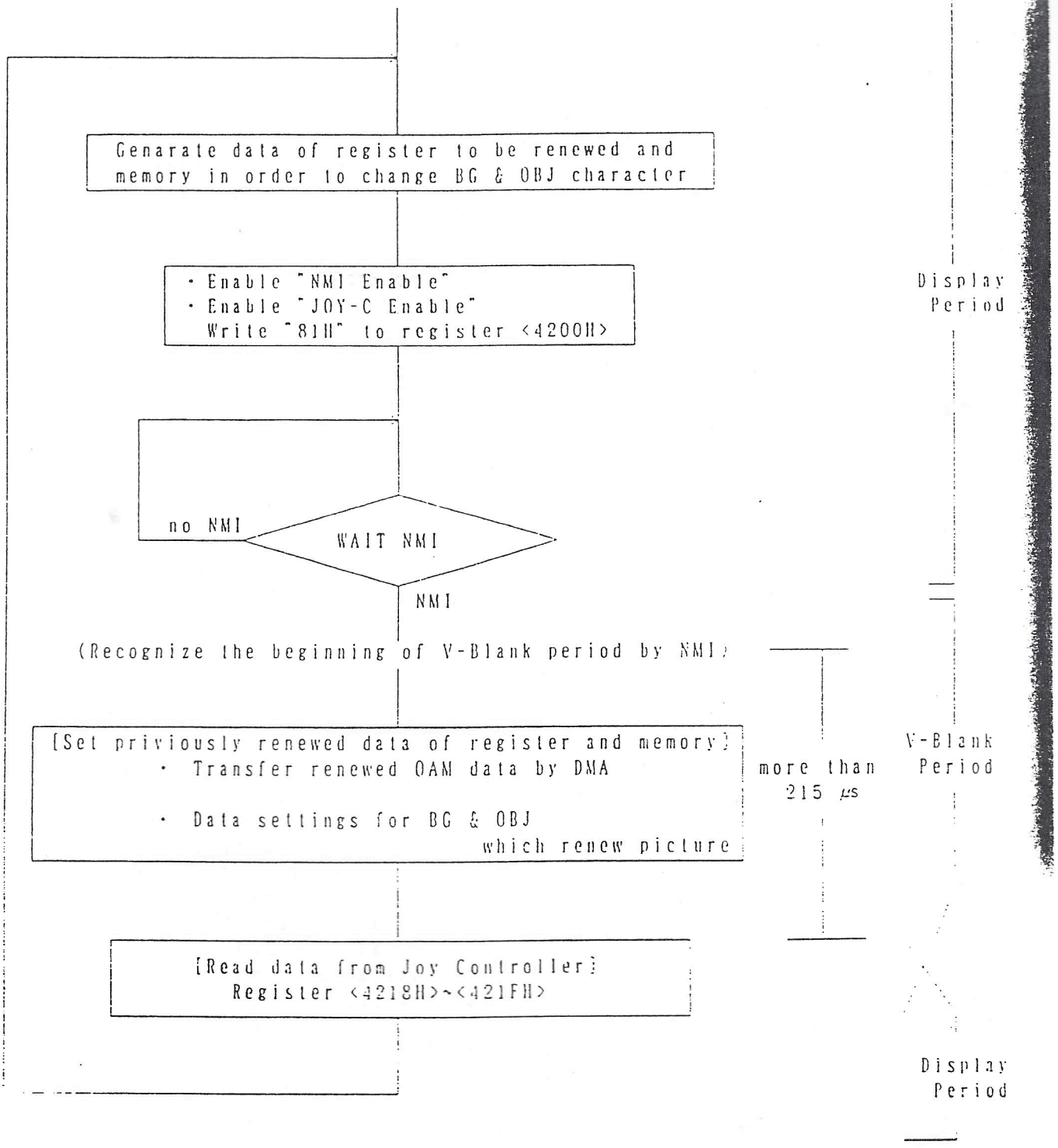
CGRAM・・・・・・・・・・ This is a Color Generator RAM (CGRAM). This is used to store color data in order to color character data.

VRAM・・・・・・・・・・・ This is a video RAM (VRAM). This is used to store character data for the background characters.

§23 SYSTEM FLOWCHART


POWER-SW ON
or
RESET-SW ON
Jump to address indicated by Reset Vector (00FFFDH, 00FFFCH)
[Forced Blank]
· Write "8FH" to register <2100H>
INITIAL SETTINGS
[Clear each Register] (See P44)
[Main Register Settings]
· Set each "Base Address"
· Set "BG Size", "BG Mode" & "BG SC Size"
· Set "OBJ Size Select" & "OBJ Name Select"
Register <2101H>, <2105H>, <2107H>~<210AH>
· THROUGH MAIN SETTINGS REGISTER <212CH>
OAM, CG RAM DATA SETTINGS
NOTE : The function to set the OAM address automatically will not work during Forced Blank period.
[OAM & CG RAM Address Settings]
· Set OAM Address
Normally write "00H" to register <2102H><2103H>
· Set CG RAM Address
Normally write "00H" to register <2121H>
Forced Blank


Transfer OAM data & CG data by using
2-channels of General purpose DMA
VRAM DATA SETTINGS
(VRAM DATA SETTINGS)
• "VRAM address H/L INC" Settings
• "VRAM address Sequence Mode" Settings
• "VRAM address" Settings
Register <2115H>,<2116H>,<2117H>
V-RAM data transfer by using General Purpose DMA
NO
OBJ. BG CHR Data
BG SC Data
has been transfered?
YES
[Register settings for initial screen to be displayed]
[Release "Forced Blank]
Write "0FH" to register <2100H> for display
Forced
Blank


Genarate data of register to be renewed and memory in order to change BG & OBJ character
・Enable "NMI Enable"
・Enable "JOY-C Enable"
Write "81H" to register <4200H>
no NMI
WAIT NMI
NMI
(Recognize the beginning of V-Blank period by NMI)
[Set priviously renewed data of register and memory]
・Transfer renewed OAM data by DMA
・Data settings for BG & OBJ which renew picture
[Read data from Joy Controller]
Register <4218H>~<421FH>
Display Period
V-Blank Period
more than 215 μs
Display Period

§ 2 4 PROGRAMMING WARNINGS

- There are registers (<210DH>～<2114H>,<211BH>～<2120H>), which must be accessed in the order of Low and High twice.
  If the number of accessing the register (write twice or read twice) becomes unknown, please initialize as follows:

OAM, CGRAM, VRAM	Set the address again
Other Registers (Write)	The lower data should be written more than one time, and the higher data should be written.
H/V Counter Read	When reading the SC78 status register <213FH> it will be initialized. The data should be read in the order of Low and High.

- The period which can be accessed for the register is as follows:

V-RAM, OAM	Forced Blank or V-Blank period only
CG-RAM	Forced Blank, V-Blank or H-Blank period only
Other Register (Write)	All period (However, when writting the data, the picture may not be displayed properly.)
Other Register (Read)	All period (However, the data which may be changed during display period may not be read properly.)

- The address space for the V-RAM is 64K-word (1-word = 16-bit) maximum. 32K-word memory is installed in the SFX unit.
- When the V-RAM is accessed from the CPU, the address counter will be increased automatically.
  For the V-RAM increment mode, please use the register mode designated by the instruction.
- When the V-RAM is read continuously after the V-RAM address has been set, the address will not be increased for the first data only. Therefore, when reading the data continuously, the first data for the address increment should be read as a dummy data after the V-RAM address has been set.
- The top color data of each CG color data palette is transparency. Because the transparency is a color which is not displayed, so that any color can be set.
  However, the color data of the CG address (00H) is normally black (background).
- Even though 9-Bit is provided as the OAM H-position, the value <100H> must not be used.

S 2 4 REGISTER CLEAR (INITIAL SETTINGS)

[Because this is a recommended settings for beginners, it is not necessary to perform according to this way.
However, the register status is not stable when power is turned on, initial settings must be done.]

ADDRESS(HEX)	DATA(HEX)
< 2 1 0 0 >	8 F (Forced Blank)
< 2 1 0 1 >	0 0
< 2 1 0 2 >	0 0
< 2 1 0 3 >	0 0
< 2 1 0 4 >	(OAM DATA)
< 2 1 0 5 >	0 0
< 2 1 0 6 >	0 0
< 2 1 0 7 >	0 0
< 2 1 0 8 >	0 0
< 2 1 0 9 >	0 0
< 2 1 0 A >	0 0
< 2 1 0 B >	0 0
< 2 1 0 C >	0 0
	(LOW) (HIGH)
< 2 1 0 D >	0 0 0 0
< 2 1 0 E >	0 0 0 0
< 2 1 0 F >	0 0 0 0
< 2 1 1 0 >	0 0 0 0
< 2 1 1 1 >	0 0 0 0
< 2 1 1 2 >	0 0 0 0
< 2 1 1 3 >	0 0 0 0
< 2 1 1 4 >	0 0 0 0
< 2 1 1 5 >	8 0
< 2 1 1 6 >	0 0
< 2 1 1 7 >	0 0
< 2 1 1 8 >	(VRAM DATA)
< 2 1 1 9 >	(VRAM DATA)
< 2 1 1 A >	0 0
< 2 1 1 B >	0 0 0 1
< 2 1 1 C >	0 0 0 0
< 2 1 1 D >	0 0 0 0
< 2 1 1 E >	0 0 0 1
< 2 1 1 F >	0 0 0 0

ADDRESS(HEX)	DATA(HEX)
< 2 1 2 0 >	0 0 0 0
< 2 1 2 1 >	0 0
< 2 1 2 2 >	(CG DATA)
< 2 1 2 3 >	0 0
< 2 1 2 4 >	0 0
< 2 1 2 5 >	0 0
< 2 1 2 6 >	0 0
< 2 1 2 7 >	0 0
< 2 1 2 8 >	0 0
< 2 1 2 9 >	0 0
< 2 1 2 A >	0 0
< 2 1 2 B >	0 0
< 2 1 2 C >	0 0
< 2 1 2 D >	0 0
< 2 1 2 E >	0 0
< 2 1 3 0 >	3 0
< 2 1 3 1 >	0 0
< 2 1 3 2 >	E 0
< 2 1 3 3 >	0 0
< 4 2 0 0 >	0 0
< 4 2 0 1 >	F F
< 4 2 0 2 >	0 0
< 4 2 0 3 >	0 0
< 4 2 0 4 >	0 0
< 4 2 0 5 >	0 0
< 4 2 0 6 >	0 0
< 4 2 0 7 >	0 0
< 4 2 0 8 >	0 0
< 4 2 0 9 >	0 0
< 4 2 0 A >	0 0
< 4 2 0 B >	0 0
< 4 2 0 C >	0 0
< 4 2 0 D >	0 0

SUPER
FAMICOM

REGISTER (PPU)

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ADDRESS : 2100H
NAME : INIDISP
CONTENTS : INITIAL SETTINGS FOR SCREEN

D7	D6	D5	D4	D3	D2	D1	D0
BLANK-ING				FADE IN/OUT (0~15)			
				F3	F2	F1	F0

2100H

└ SCREEN BRIGHTNESS : Determine the Screen Brightness (16-Stages)

F3	F2	F1	F0	BRIGHTNESS
1	1	1	1	BRIGHT
1	1	1	0	↓
		↓		
0	0	0	0	DARK

└ BLANKING : FORCED BLANKING ┌ 0 : NON-BLANKING
└ 1 : BLANKING

ADDRESS : 2101H
NAME : OBJSEL
CONTENTS : OBJECT SIZE & OBJECT DATA AREA DESIGNATION

D7	D6	D5	D4	D3	D2	D1	D0
OBJ SIZE SELECT			OBJ NAME SELECT		OBJ NAME BASE SELECT		
S2	S1	S0	N1	N0	BA-2	BA-1	BA-0

2101H

└ OBJECT BASE ADDRESS (UPPER-3 BIT)
: Designate the segment (8K-word/segment) address which the OBJ data is stored in the VRAM. (See Appendix-1 & 2)

└ OBJECT DATA AREA SELECT
: The upper 4K-word out of the area (8K-word) designated by "Object Base Address" is assigned as the Base Area. and the area of the lower 4K-word combined with its Base Area can be selected. (See Appendix-1 & 2)

└ OBJECT SIZE : DESIGNATE OBJECT SIZE (See Appendix-3 & 4)

S2	S1	S0	OBJ SIZE 0	OBJ SIZE 1
0	0	0	8 DOT	16 DOT
0	0	1	8 DOT	32 DOT
0	1	0	8 DOT	64 DOT
0	1	1	16 DOT	32 DOT
1	0	0	16 DOT	64 DOT
1	0	1	32 DOT	64 DOT

(SIZE LARGE/SMALL)

ADDRESS : 2102H / 2103H
NAME : OAMADDL /OAMADDH
CONTENTS : ADDRESS FOR ACCESSING OAM (OBJECT ATTRIBUTE MEMORY)

ADDRESS

D7	D6	D5	D4	D3	D2	D1	D0	
OAM ADDRESS								2102H
A7	A6	A5	A4	A3	A2	A1	A0	

OAM PRIORITY ROTATION		OAM ADDRESS MSB A8	2103H

- This is the INITIAL ADDRESS to be set in advance when reading from the OAM or writting to the OAM.
- By writing "1" to D7 (OAM Priority Rotation) of register <2103H> and setting the OAM address. the OBJ for the address set has highest priority.
- The address which has been set just before every field (beginning of V-BLANK) will be set again to registers <2102H> <2103H> automatically.
  But, the address can not be set automatically during Forced Blank period.

ADDRESS : 2104H
NAME : OAM DATA
CONTENTS : DATA FOR OAM WRITE

D7	D6	D5	D4	D3	D2	D1	D0	
OAM DATA (LOW, HIGH)								2104H
D7	D6	D5	D4	D3	D2	D1	D0	

- This is the OAM data to be written at any address of the OAM. (See Appendix-3)
- After register <2102H> or <2103H> is accessed. the data must be written in the order of Lower 8-Bit & Upper 8-Bit of register <2104H>.
  The OAM address will be increased automatically when the OAM data is written in the order of LOW & HIGH.
- The data can be written only during V-BLANK or FORCED BLANK period.

ADDRESS : 2105H
NAME : BGMODE
CONTENTS : BG MODE & CHARACTER SIZE SETTINGS

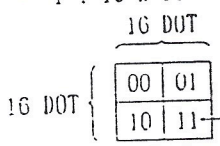
D7	D6	D5	D4	D3	D2	D1	D0
BG SIZE				BG3	BG MODE		
BG4	BG3	BG2	BG1	PRIO.	M2	M1	M0

2105H

BG SCREEN MODE SELECT : See BG Screen Mode Summary (See Appendix-5)

HIGHEST PRIORITY DESIGNATION FOR BG-3 : Make BG3 highest priority
- 0 : OFF (See Appendix-16)
- 1 : ON

BG SIZE DESIGNATION : Designate the size for each BG Character (See Appendix-18 & 19)
- 0 : 8 x 8 DOT/CHARACTER
- 1 : 16 x 16 DOT/CHARACTER



ADDRESS : 2106H
NAME : MOSAIC
CONTENTS : SIZE & SCREEN DESIGNATION FOR MOSAIC DISPLAY

D7	D6	D5	D4	D3	D2	D1	D0
MOSAIC SIZE				MOSAIC ENABLE			
M3	M2	M1	M0	BG4	BG3	BG2	BG1

2106H

MOSAIC MODE SELECT : ON/OFF for Mosaic Mode of each BG
- 0 : OFF
- 1 : ON

MOSAIC MODE SIZE DESIGNATION : DESIGNATE MOSAIC MODE SIZE (SEE APPENDIX-6)

256 MODE

M3	M2	M1	M0	SIZE
0	0	0	0	1 x 1 DOT
0	0	0	1	2 x 2 DOT
0	0	1	0	3 x 3 DOT
		:		:
1	1	1	0	15x15 DOT
1	1	1	1	16x16 DOT

512 MODE H x V

M3	M2	M1	M0	SIZE (H:NON-INTERLACE)
0	0	0	0	2 x 2 DOT (2 x 1 DOT)
0	0	0	1	4 x 4 DOT (4 x 2 DOT)
0	0	1	0	6 x 6 DOT (6 x 3 DOT)
		:		
1	1	1	0	30×30 DOT (30×15 DOT)
1	1	1	1	32×32 DOT (32×16 DOT)

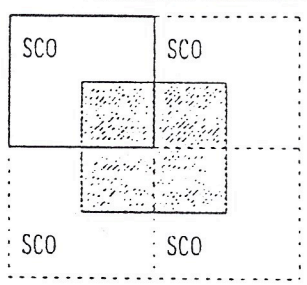
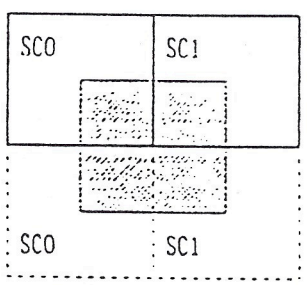
ADDRESS : 2107H / 2108H / 2109H / 210AH
NAME : BG1SC / BG2SC / BG3SC / BG4SC
CONTENTS : ADDRESS FOR STORING SC-DATA OF EACH BG & SC SIZE DESIGNATION (MODE 0 ~6)

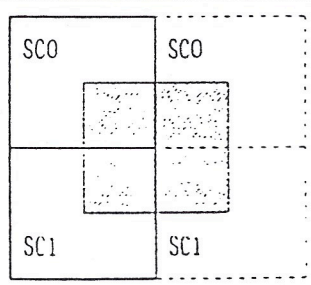
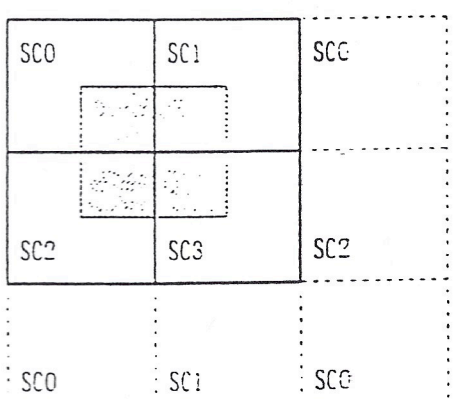
D7	D6	D5	D4	D3	D2	D1	D0	
BG1 SC BASE ADDRESS						BG1 SC SIZE		2107H
A5	A4	A3	A2	A1	A0	S1	S0	
BG2 SC BASE ADDRESS						BG2 SC SIZE		2108H
A5	A4	A3	A2	A1	A0	S1	S0	
BG3 SC BASE ADDRESS						BG3 SC SIZE		2109H
A5	A4	A3	A2	A1	A0	S1	S0	
BG4 SC BASE ADDRESS						BG4 SC SIZE		210AH
A5	A4	A3	A2	A1	A0	S1	S0	

SCREEN SIZE DESIGNATION (See Appendix-13 & 19)
: Designate Background Screen Size

BACKGROUND SCREEN BASE ADDRESS (UPPER 6-BIT)
: Designate the segment which BG-SC data in the VRAM is stored.
(1K-WORD/SEGMENT)

SCREEN SIZE & SCREEN REPETITION

S1	S0	SCREEN SIZE
0	0	
0	1	

S1	S0	SCREEN SIZE
1	0	
1	1	

ADDRESS : 210BH / 210CH
NAME : BG12NBA / BG34NBA
CONTENTS : BG CHARACTER DATA AREA DESIGNATION

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
BG 2 NAME BASE ADDRESS				BG 1 NAME BASE ADDRESS				210BH
A3	A2	A1	A0	A3	A2	A1	A0	

BG 4 NAME BASE ADDRESS				BG 3 NAME BASE ADDRESS				210CH
A3	A2	A1	A0	A3	A2	A1	A0	

BACKGROUND NAME BASE ADDRESS (UPPER 4-BIT)
: Designate the segment address in the VRAM which BG character data is stored.
(4K-WORD/SEGMENT)

ADDRESS : 210DH / 210EH
NAME : BG1HOFS / BG1VOFS
CONTENTS : H/V SCROLL VALUE DESIGNATION FOR BG-1

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
BG 1 H-OFFSET (LOW, HIGH)								
			(H012)	(H011)	(H010)	(H0 9)	(H0 8)	210DH
H0 7	H0 6	H0 5	H0 4	H0 3	H0 2	H0 1	H0 0	

BG 1 V-OFFSET (LOW, HIGH)								
			(V012)	(V011)	(V010)	(V0 9)	(V0 8)	210EH
V0 7	V0 6	V0 5	V0 4	V0 3	V0 2	V0 1	V0 0	

- 10-Bit maximum (0 ~ 1023) can be designated for H/V scroll value.
  (The size of 13-bit maximum (-4096~4095) can be designated in MODE-7) (See Appendix-8 & 9)
- By writing to the register twice, the data can be set in the order of Low and High.

ADDRESS : 210F H / 2110 H / 2111 H / 2112 H / 2113 H / 2114 H
NAME : BG2HOFS / BG2VOFS / BG3HOFS / BG3VOFS / BG4HOFS / BG4VOFS
CONTENTS : H/V SCROLL VALUE DESIGNATION FOR BG-2. 3. 4

D7	D6	D5	D4	D3	D2	D1	D0	
BG H-OFFSET (LOW, HIGH)								210FH
						(H0 9)	(H0 8)	2111H
H0 7	H0 6	H0 5	H0 4	H0 3	H0 2	H0 1	H0 0	2113H
BG V-OFFSET (LOW, HIGH)								2110H
						(V0 9)	(V0 8)	2112H
V0 7	V0 6	V0 5	V0 4	V0 3	V0 2	V0 1	V0 0	2114H

- 10 bit maximum (0~1023) of the H/V scroll value can be designated. (See Appendix-8)
- By writing to the register twice. the data can be set in the order of Low and High.

ADDRESS : 2115H
NAME : VMAINC
CONTENTS : VRAM ADDRESS INCREMENT VALUE DESIGNATION

D7	D6	D5	D4	D3	D2	D1	D0	
H/L				V-RAM ADDRESS SEQUENCE MODE				210BH
				FULL GRAPHIC		SC INCREMENT		
INC				G1	G0	I1	I0	

Designate the increment value for the VRAM address
(See Appendix-7)

G1	G0	I1	I0	INCREMENT VALUE
0	1	0	0	Increment by 8 for 32 times (2-Bit Formation)
1	0	0	0	Increment by 8 for 64 times (4-Bit Formation)
1	1	0	0	Increment by 8 for 128 times (8-Bit Formation)
0	0	0	0	Address Increments 1 BY 1
0	0	0	1	Address Increments 32 BY 32
0	0	1	0	Address Increments 64 BY 64
0	0	1	1	Address Increments 128 BY 128

Designate the increment timing for the address
- 0 : The address will be increased after the data has been written to register <2119H> or the data has been read from register <2139H>.
- 1 : The address will be increased after the data has been written to register <2119H> or the data has been read from register <213AH>.

ADDRESS : 2116H / 2117H
NAME : VMADDL / VMADDH
CONTENTS : ADDRESS FOR VRAM READ

D7	D6	D5	D4	D3	D2	D1	D0	
VRAM ADDRESS (LOW)								2116H
A7	A6	A5	A4	A3	A2	A1	A0	
VRAM ADDRESS (HIGH)								2117H
A15	A14	A13	A12	A11	A10	A9	A8	

- This is the initial address for reading from the VRAM or writing to the VRAM.
- The data is read or written by the address set initially, and every time the data is read, the address will be increased automatically.
- The value to be increased is determined by "SC INCREMENT" of register <2115H> and the setting value of the "FULL GRAPHIC".

ADDRESS : 2118H / 2119H
NAME : VMDATAL / VMDATAH
CONTENTS : DATA FOR VRAM WRITE

D7	D6	D5	D4	D3	D2	D1	D0	
VRAM DATA (LOW)								2118H
A7	A6	A5	A4	A3	A2	A1	A0	
VRAM DATA (HIGH)								2119H
A15	A14	A13	A12	A11	A10	A9	A8	

- This is the screen data and character data (BG & OBJ), which can write at any address of the VRAM.
- According to the settings of register <2115H> "H/L INC", the data can be written to the VRAM as follows:

H/L INC	WRITE TO REGISTER	OPERATION
0	Write to <2118H> only	The Data is written to lower 8-bit of the VRAM and the address will be increased automatically.
1	Write to <2119H> only	The Data is written to upper 8-bit of the VRAM and the address will be increased automatically.
0	Write in the order of <2119H> & <2118H>	When the data is set in the order of upper & lower the address will be increased.
1	Write in the order of <2118H> & <2119H>	When the data is set in the order of lower & upper the address will be increased.

NOTE : The data can be written only during V-BLANK or FORCED BLANK period.

ADDRESS : 211AH
NAME : M7SEL
CONTENTS : INITIAL SETTING IN SCREEN MODE-7

D7	D6	D5	D4	D3	D2	D1	D0
SCREEN OVER						SCREEN FLIP	
01	00					V	H

211AH

HORIZONTAL/VERTICAL FLIP
: H-FLIP/V-FLIP in the Screen Mode-7

V	H	DISPLAY
0	0	Normal display
0	1	H-Directional Flip only
1	0	V-Directional Flip only
1	1	Both H & V Directional Flip

The following process is made if the screen to be displayed is outside of the screen area.

01	00	PROCESS OUT OF AREA
0	0	Screen repetition if outside of screen area
1	0	Character # repetition if outside of screen area
1	1	Outside of the screen area is the Back Drop Screen in single color

ADDRESS : 211B H / 211C H / 211D H / 211E H / 211F H / 2120 H
NAME : M7A / M7B / M7C / M7D / M7X / M7Y
CONTENTS : ROTATION/ENLARGEMENT/REDUCTION IN MODE-7. CENTER COORDINATE SETTINGS
MULTIPLICAND/MULTIPLIER SETTINGS OF COMPLEMENTARY MULTIPLICATION

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
MATRIX PARAMETER A (LOW, HIGH)								
(MP15)	(MP14)	(MP13)	(MP12)	(MP11)	(MP10)	(MP 9)	(MP 8)	211BH
MP 7	MP 6	MP 5	MP 4	MP 3	MP 2	MP 1	MP 0	
MATRIX PARAMETER B (LOW, HIGH)								
(MP15)	(MP14)	(MP13)	(MP12)	(MP11)	(MP10)	(MP 9)	(MP 8)	211CH
MP 7	MP 6	MP 5	MP 4	MP 3	MP 2	MP 1	MP 0	
MATRIX PARAMETER C (LOW, HIGH)								
(MP15)	(MP14)	(MP13)	(MP12)	(MP11)	(MP10)	(MP 9)	(MP 8)	211DH
MP 7	MP 6	MP 5	MP 4	MP 3	MP 2	MP 1	MP 0	
MATRIX PARAMETER D (LOW, HIGH)								
(MP15)	(MP14)	(MP13)	(MP12)	(MP11)	(MP10)	(MP 9)	(MP 8)	211EH
MP 7	MP 6	MP 5	MP 4	MP 3	MP 2	MP 1	MP 0	

- The 8-bit data should be written twice in the order of lower and upper. The rotation, enlargement and reduction should be set by its 16-bit data.
- The value down to a decimal point should be set to the lower 8-bit. The most upper 8-bit is for the signed bit. (MP15 is the signed bit. There is a deci
- FORMULA FOR ROTAION/ENLARGEMENT/REDUCTION (See Appendix-13)

$$\begin{pmatrix} X_2 \\ Y_2 \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \begin{pmatrix} X_1 - X_0 \\ Y_1 - Y_0 \end{pmatrix} + \begin{pmatrix} X_0 \\ Y_0 \end{pmatrix}$$

$A = \cos\gamma \times (1/\alpha)$, $B = \sin\gamma \times (1/\alpha)$, $C = -\sin\gamma \times (1/\beta)$, $D = \cos\gamma \times$
γ : Rotation Angle α : Reduction Rates for X(H) β : Reduction Rates
$X_0 \cdot Y_0$: Center Coordinate. $X_1 \cdot Y_1$: Display Coordinate.
$X_2 \cdot Y_2$: Coordinate before Calculation

- Set the value of "A" to the register <211BH>. In the same way, set "B <211CH> ~<211EH>.

* The complementary multiplication (16-bit x 8-bit) can be done by using reg
When setting 16-bit data to register <211BH> and 8-bit data to register <2
the multiplication result can be indicated rapidly by reading registers <2

d 7	d 6	d 5	d 4	d 3	d 2	d 1	d 0	
CENTER POSITION X_0 (LOW, HIGH)								
			(X12)	(X11)	(X10)	(X9)	(X8)	211FH
X7	X6	X5	X4	X3	X2	X1	X0	
CENTER POSITION Y_0 (LOW, HIGH)								
			(Y12)	(Y11)	(Y10)	(Y9)	(Y8)	2120H
Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	

- The center coordinate (X_0, Y_0) for Rotation/Enlargement/Reduction can this register.
- The coordinate value of X_0 & Y_0 can be designated by 13-bit complement
- This register requires that the lower 8-bit is set first and the upper 5- Therefore, 13-bit data in total can be set.

ADDRESS : 211B H / 211C H / 211D H / 211E H / 211F H / 2120 H
NAME : M7A / M7B / M7C / M7D / M7X / M7Y
CONTENTS : ROTATION/ENLARGEMENT/REDUCTION IN MODE-7. CENTER COORDINATE SETTINGS & MULTIPLICAND/MULTIPLIER SETTINGS OF COMPLEMENTARY MULTIPLICATION

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
MATRIX PARAMETER A (LOW, HIGH)								
(MP15)	(MP14)	(MP13)	(MP12)	(MP11)	(MP10)	(MP 9)	(MP 8)	211BH
MP 7	MP 6	MP 5	MP 4	MP 3	MP 2	MP 1	MP 0	
MATRIX PARAMETER B (LOW, HIGH)								
(MP15)	(MP14)	(MP13)	(MP12)	(MP11)	(MP10)	(MP 9)	(MP 8)	211CH
MP 7	MP 6	MP 5	MP 4	MP 3	MP 2	MP 1	MP 0	
MATRIX PARAMETER C (LOW, HIGH)								
(MP15)	(MP14)	(MP13)	(MP12)	(MP11)	(MP10)	(MP 9)	(MP 8)	211DH
MP 7	MP 6	MP 5	MP 4	MP 3	MP 2	MP 1	MP 0	
MATRIX PARAMETER D (LOW, HIGH)								
(MP15)	(MP14)	(MP13)	(MP12)	(MP11)	(MP10)	(MP 9)	(MP 8)	211EH
MP 7	MP 6	MP 5	MP 4	MP 3	MP 2	MP 1	MP 0	

- The 8-bit data should be written twice in the order of lower and upper. Then, the parameter of rotation, enlargement and reduction should be set by its 16-bit data.
- The value down to a decimal point should be set to the lower 8-bit. The most significant bit of the upper 8-bit is for the signed bit. (MP15 is the signed bit. There is a decimal point between M7 & M8
- FORMULA FOR ROTAION/ENLARGEMENT/REDUCTION (See Appendix-13)

$$\begin{pmatrix} X_2 \\ Y_2 \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \begin{pmatrix} X_1 - X_0 \\ Y_1 - Y_0 \end{pmatrix} + \begin{pmatrix} X_0 \\ Y_0 \end{pmatrix}$$

$A = \cos\gamma \times (1/\alpha)$, $B = \sin\gamma \times (1/\alpha)$, $C = -\sin\gamma \times (1/\beta)$, $D = \cos\gamma \times (1/\beta)$
γ : Rotation Angle α : Reduction Rates for X(H) β : Reduction Rates for Y(V)
$X_0 \cdot Y_0$: Center Coordinate. $X_1 \cdot Y_1$: Display Coordinate.
$X_2 \cdot Y_2$: Coordinate before Calculation

- Set the value of "A" to the register <211BH>. In the same way, set "B~D" to the register <211CH> ~<211EH>.

* The complementary multiplication (16-bit x 8-bit) can be done by using regidters <211BH> <211CH>. When setting 16-bit data to register <211BH> and 8-bit data to register <211CH>, the multiplication result can be indicated rapidly by reading registers <2134H> ~<2136H>.

d 7	d 6	d 5	d 4	d 3	d 2	d 1	d 0	
CENTER POSITION X_0 (LOW, HIGH)								
			(X12)	(X11)	(X10)	(X9)	(X8)	211FH
X7	X6	X5	X4	X3	X2	X1	X0	
CENTER POSITION Y_0 (LOW, HIGH)								
			(Y12)	(Y11)	(Y10)	(Y9)	(Y8)	2120H
Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	

- The center coordinate (X_0, Y_0) for Rotation/Enlargement/Reduction can be designated by this register.
- The coordinate value of X_0 & Y_0 can be designated by 13-bit complement of 2.
- This register requires that the lower 8-bit is set first and the upper 5-bit is set. Therefore, 13-bit data in total can be set.

ADDRESS : 2121H
NAME : CGADD
CONTENTS : ADDRESS FOR CG-RAM WRITE

D7	D6	D5	D4	D3	D2	D1	D0	
CG RAM ADDRESS								2121H
A7	A6	A5	A4	A3	A2	A1	A0	

- This is the initial address for reading from the CG-RAM or writing to the CG-RAM
- The data is read by the address set initially. and every time the data is read or written. the address will be increased automatically.

ADDRESS : 2122H
NAME : CGDATA
CONTENTS : DATA FOR CG-RAM WRITE

D7	D6	D5	D4	D3	D2	D1	D0	
CG RAM DATA (LOW. HIGH)								2122H
(D14)	(D13)	(D12)	(D11)	(D10)	(D9)	(D8)		
D7	D6	D5	D4	D3	D2	D1	D0	

- This is the color generater data to be written at any address of the CG-RAM.
- The mapping of BG1~BG4 and OBJ data in the CG-RAM will be determined. which is performed by every mode selected by "BG MODE" of register <2105H>. (See Appendix-14)
- There are the color data of 8-palettes for each screen of BG1 ~ BG4. The palette selection is determined by 3-bit of the SC data "COLOR".
- Because the CG-RAM data is 15-bit/word. it is necessary to set lower 8-bit first to this register and then upper 7-bit should be set. When both lower and upper are set. the address will be increased by 1 automatically.

NOTE : After the address is set. the data should be written from the lower as well as the OAM.

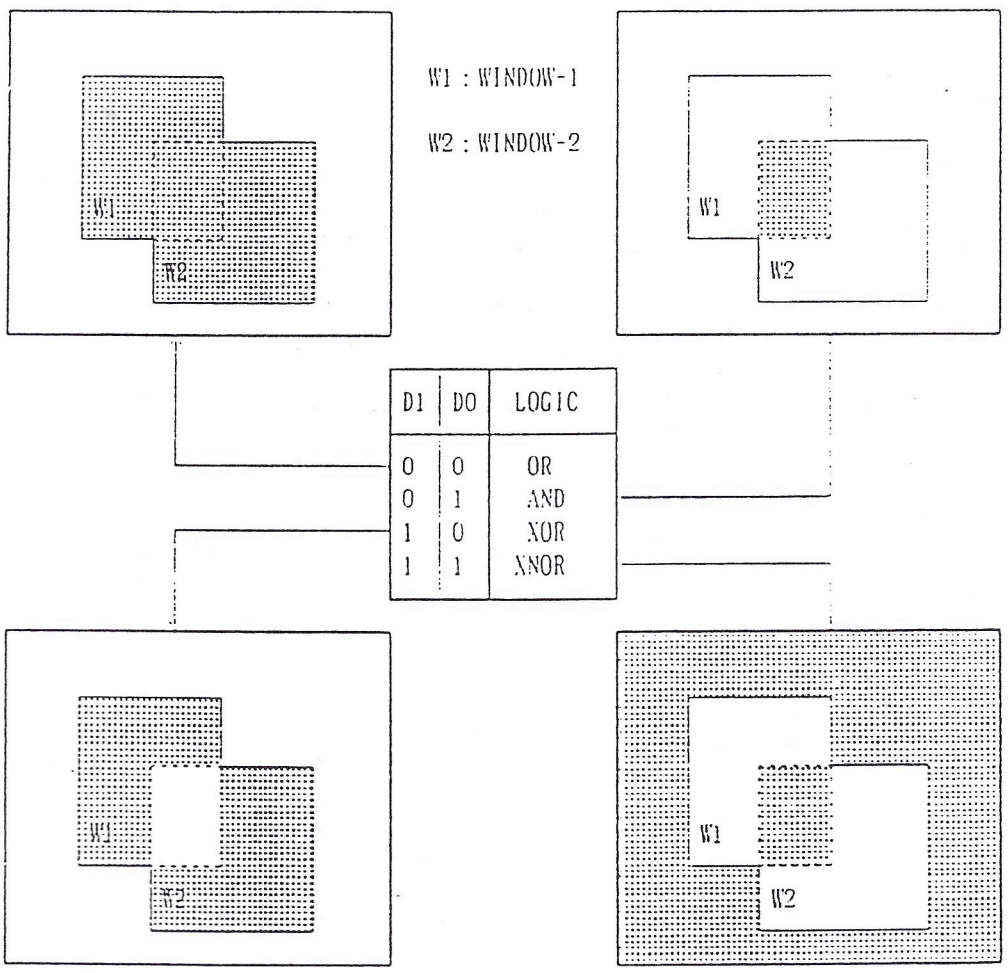
NOTE : The data can be written only during H/V BLANK or FORCED BLANK period.

ADDRESS : 212AH / 212BH
NAME : WBGLOG / WOBJLOG
CONTENTS : MASK LOGIC SETTINGS FOR WINDOW-1 & 2 ON EACH SCREEN

D7	D6	D5	D4	D3	D2	D1	D0	
WINDOW LOGIC								212AH
BG4		BG3		BG2		BG1		
D1	D0	D1	D0	D1	D0	D1	D0	
				WINDOW LOGIC				212BH
				Color		OBJ		
				D1	D0	D1	D0	

WINDOW LOGIC : SET MASK LOGIC FOR WINDOW-1 & 2

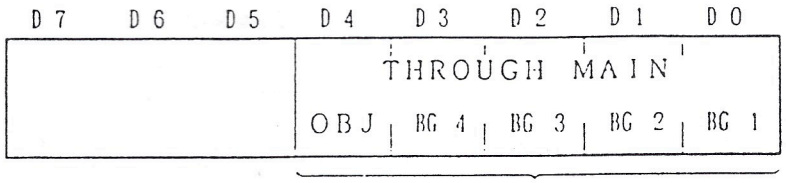
When both window-1 and window-2 are "IN", the shaded portion will be masked as follows:



D1	D0	LOGIC
0	0	OR
0	1	AND
1	0	XOR
1	1	XNOR

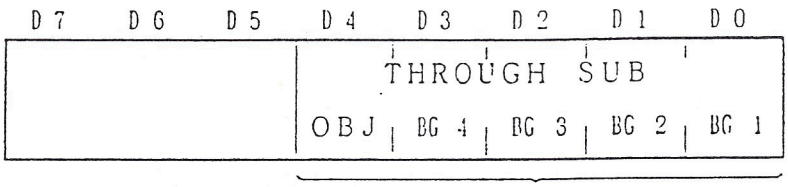
NOTE : "IN/OUT" of registers <2123H> <2124H> <2125H> becomes the "NOT logic" for each window-1 and window-2.

ADDRESS : 212CH
NAME : TM
CONTENTS : MAIN SCREEN DESIGNATION



MAIN SCREEN DESIGNATION
: Designate the screen (BG1 ~ BG4, OBJ) to be displayed as the Main Screen.
Designate the screen to be added for the screen addition/subtraction
0 : DISABLE
1 : ENABLE

ADDRESS : 212DH
NAME : TS
CONTENTS : SUB SCREEN DESIGNATION



SUB SCREEN DESIGNATION
: Designate the screen (BG1 ~ BG4, OBJ) to be displayed as SUB-Screen.
Designate the addition subtraction screen at the point when the screen addition subtraction is functioning.
0 : DISABLE
1 : ENABLE

※ When the screen addition/subtraction is functioning, the SUB screen is a screen to be added or subtracted against the MAIN screen.

ADDRESS : 212EH
NAME : TMW
CONTENTS : WINDOW MASK DESIGNATION FOR MAIN SCREEN

D7	D6	D5	D4	D3	D2	D1	D0	
			THROUGH		MAIN		(WINDOW)	212EH
			OBJ	BG4	BG3	BG2	BG1	

WINDOW MASK DESIGNATION FOR MAIN SCREEN
: In the window area designated by register <2123H> ~ <2129H>. the screen to be displayed can be designated. which is selected among the Main screen designated by register <212CH>.
0 : DISABLE
1 : ENABLE

ADDRESS : 212FH
NAME : TSW
CONTENTS : WINDOW MASK DESIGNATION FOR SUB SCREEN

D7	D6	D5	D4	D3	D2	D1	D0	
			THROUGH		SUB		(WINDOW)	212FH
			OBJ	BG4	BG3	BG2	BG1	

WINDOW MASK DESIGNATION FOR SUB SCREEN
: In the window area designated by register <2123H> ~ <2129H>. the screen to be displayed can be designated. which is selected among the Sub screen designated by register <212CH>.
0 : DISABLE
1 : ENABLE

※ When the screen addition subtraction is functioning. the SUB screen is a screen to be added or subtracted against the MAIN screen.

ADDRESS : 2130H
NAME : CGSWSEL
CONTENTS : INITIAL SETTINGS FOR FIXED COLOR ADDITION OR SCREEN ADDITION

D7	D6	D5	D4	D3	D2	D1	D0
COLOR WINDOW ON/OFF MAIN SW (A)		SUB SW (B)				CC ADD ENABLE	DIRECT SELECT
M1	M0	S1	S0				

2130H

DIRECT SELECT (See Appendix-14)
: The VRAM data (Color and Character data) become the color data directly. (Only when mode-3, 4 & 7 are selected.)
0 : DISABLE
1 : ENABLE

COLOR WINDOW ON/OFF MAIN/SUB SWITCH
: When the Color Window is functioning, the assignment of the window area for MAIN and SUB screen can be designated.

FIXED COLOR ADDITION/SUBTRACTION ENABLE
: Designate whether 2 kinds of the data should be added/subtracted each other or not, which are the fixed color set by register <2132H> and the color data which is set to the CGRAM.
0 : ADDITION/SUBTRACTION FOR FIXED COLOR
1 : ADDITION/SUBTRACTION FOR SUB SCREEN

M1(S1)	M0(S0)	FUNCTION
0	0	ON (All the time)
0	1	ON (inside window only)
1	0	ON (outside window only)
1	1	OFF (All the time)

ADDRESS : 2131H
NAME : CGADSUB
CONTENTS : ADDITION/SUBTRACTION & SUBTRACTION DESIGNATION FOR EACH SCREEN, OBJ & BACKGROUND COLOR

D7	D6	D5	D4	D3	D2	D1	D0
ADD SUB	1/2 ENABLE	ADD or SUB ENABLE					
		BACK	OBJ	BG 4	BG 3	BG 2	BG 1

2131H

COLOR DATA ADDITION/SUBTRACTION ENABLE
: Designate the selection either of the disable or the enable for the addition/subtraction of the fixed color data or the screen color data.
0 : DISABLE
1 : ENABLE (Addition/Subtraction function : ON)

NOTE : In case the OBJ is designated, the Addition Subtraction function is available only when the OBJ color palette is either 6 or 7.

"1/2 OF COLOR DATA" DESIGNATION : When the color constant addition/subtraction or the screen addition/subtraction is performed, designate whether the RGB result in the addition/subtraction area should be "1/2" or not. However, in the back (color constant) area on the Sub screen, it does not become "1/2".
0 : DISABLE
1 : ENABLE ("1/2" function : ON)

COLOR DATA ADDITION/SUBTRACTION SELECT: Designate the selection either of the addition or the subtraction mode.
0 : ADDITION MODE SELECT
1 : SUBTRACTION MODE SELECT

ADDRESS : 2132H
NAME : COLDATA
CONTENTS : FIXED COLOR DATA FOR FIXED COLOR ADDITION/SUBTRACTION

D7	D6	D5	D4	D3	D2	D1	D0	
COLOR CONSTANT DATA								2132H
COLOR DESIGNATION			COLOR BRILLIANCE DATA					
BLUE	GREEN	RED	D4	D3	D2	D1	D0	

COLOR CONSTANTOR DATA : Set the color constant data for color constant addition/subtraction

COLOR DESIGNATION : BIT FOR SELECTING DESIRED COLOR

- R/G/B brightness should be set by the data of each 5-Bit.

[EXAMPLE]
RED : C0H, 3FH (B=00H, G=00H, R=1FH)
GREEN : A0H, 5FH (B=00H, G=1FH, R=00H)
BLUE : 60H, 9FH (B=1FH, G=00H, R=00H)
WHITE : FFH
BLACK : E0H

ADDRESS : 2133H
NAME : SETINI
CONTENTS : SCREEN INITIAL SETTING

D7	D6	D5	D4	D3	D2	D1	D0	
EXT. SYNC.	EXT. INPUT			PSEUDO 512	224/239	OBJ-V SELECT	INTER-LACE	2133H

SCANNING : INTERLACE/NON-INTERLACE SELECTION
(It relates to <2105H>)
0 : NON-INTERLACE
1 : INTERLACE

OBJ V-DIRECTION DISPLAY
: In the interlace mode, select either of 1-dot per line or 1-dot repeated every 2 lines. If "1" is written, the OBJ seems to be reduced half vertically in appearance.
(If "1" is set other than the interlace mode, even-numbered line and odd-numbered line of the OBJ will be dusplayed alternately every field.)

BG V-DIRECTION DISPLAY : Switch the display line of a field to 224-Line or 239-Line.
(In case of interlace mode, it will be doubled dot.)
0 : 224 LINE
1 : 239 LINE

HORIZONTAL PSEUDO 512 MODE : 512 imaginary resolution (Horizontal can be made by shifting the SUB screen half dot to the left alternately every field.
0 : DISABLE
1 : ENABLE

EXTBG MODE (SCREEN EXPAND) : Enable the data supplied from the external LSI. For the SFX, enable when the screen with priority is used on mode-7.

EXTERNAL SYNCHRONIZATION : It is used for super-impose and etc. Normally, "0" should be written.

ADDRESS : 2134H / 2135H / 2136H
NAME : #MPYL / #MPYM / #MPYH
CONTENTS : MULTIPLICATION RESULT

D7	D6	D5	D4	D3	D2	D1	D0	
MPY (LOW)								2134H
M7	M6	M5	M4	M3	M2	M1	M0	
MPY (MID)								2135H
M15	M14	M13	M12	M11	M10	M9	M8	
MPY (HIGH)								2136H
M23	M22	M21	M20	M19	M18	M17	M16	

- This is a Multiplication result (complement of 2) can be read by setting 16-bit to register <211BH> and setting 8-Bit data to register <211CH>.

ADDRESS : 2137H
NAME : #SLHV
CONTENTS : SOFTWARE LATCH FOR H/V COUNTER

D7	D6	D5	D4	D3	D2	D1	D0	
SOFT LATCH FOR H/V COUNTER								2137H
SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0	

- This is a register, which generate the pulse for latching the H/V counter value.
- The H/V counter value at the point when register <2137H> is read can be latched. The data which was read is meaningless data.
- The H/V counter value latched can be reffered by registers <213CH> <213DH>.

ADDRESS : 2138H
NAME : #OAMDATA
CONTENTS : READ DATA FROM OAM

D7	D6	D5	D4	D3	D2	D1	D0
OAM DATA (LOW, HIGH)							
D7	D6	D5	D4	D3	D2	D1	D0

2138H

- This is a register, which can read the data at any address of the OAM.
- When the address is set to register <2102H><2103H> and register <2138H> is also accessed. the data can be read in the order of Low 8-bit/High 8-bit. Afterward, the address will be increased automatically, and the data of the next address can be read.

NOTE : The data can be read only during H/V BLANK or FORCED BLANK period.

ADDRESS : 2139H / 213AH
NAME : #VMDATAL / #VMDATAH
CONTENTS : READ DATA FROM VRAM

D7	D6	D5	D4	D3	D2	D1	D0
VRAM DATA (LOW)							
D7	D6	D5	D4	D3	D2	D1	D0

2139H

VRAM DATA (HIGH)							
D15	D14	D13	D12	D11	D10	D9	D8

213AH

- This is a register, which can read the data at any address of the VRAM.
- The initial address should be set by registers <2116H> and <2117H>. The data can be read by the address which has been set initially.
- When reading the data continuously, the first data for the address increment should be read as a dummy data after the address has been set.
- Quantity to be increased will be determined by "SC INCREMENT" of register <2115H> and the setting value of the "FULL GRAPHIC"

NOTE : The data can be read only during H/V BLANK or FORCED BLANK period.

ADDRESS : 213BH
NAME : *CGDATA
CONTENTS : READ DATA FROM CG-RAM

D7	D6	D5	D4	D3	D2	D1	D0	
CG DATA (LOW. HIGH)								
(D14)	(D13)	(D12)	(D11)	(D10)	(D9)	(D8)		213BH
D7	D6	D5	D4	D3	D2	D1	D0	

- This is a register. which can read the data at any address of the CG-RAM.
- The initial address can be set by register <2121H>. The lower 8-bit is read first. and then the upper 7-bit will be read by accessing this register. The current address will be increased to the next address at the same time the upper 7-bit is read.

NOTE : The data can be read only during H/V BLANK or FORCED BLANK period.

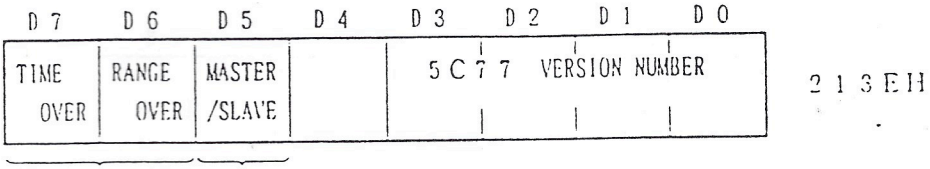
ADDRESS : 213CH / 213DH
NAME : *OPHCT / *OPVCT
CONTENTS : H/V COUNTER DATA BY EXTERNAL OR SOFTWARE LATCH

D7	D6	D5	D4	D3	D2	D1	D0	
OUTPUT DATA OF H-COUNTER								
							(H8)	213CH
H7	H6	H5	H4	H3	H2	H1	H0	

OUTPUT DATA OF V-COUNTER								
							(V8)	213DH
V7	V6	V5	V4	V3	V2	V1	V0	

- The H/V counter is latched by reading register <2137H>. and its H/V counter value can be read by this register.
- The H/V counter is also latched by the external latch. and its value can be read by this register.
- If register <213CH> or <213DH> is read after register <213FH> has been read. the lower 8-bit data will be read first. and then the upper 1-bit will be read by reading the register.

ADDRESS : 213EH
NAME : *STAT77
CONTENTS : PPU STATUS FLAG & VERSION NUMBER

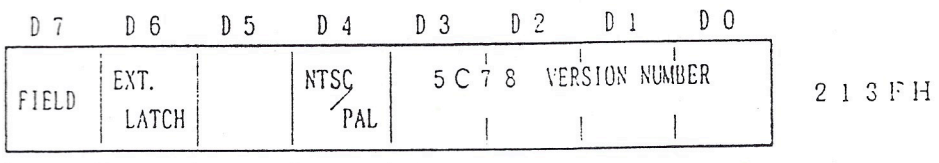


MASTER / SLAVE MODE SELECT : LSI MODE (Normally "0" is set)

OBJ DISPLAY STATUS (ON A HORIZONTAL LINE)
- RANGE : When Quantity of the OBJ (regardless of the size) becomes 33 pcs or more. "1" will be set.
- TIME : When quantity of the OBJ which is converted to "8 X 8-SIZE" is 35 pcs or more. "1" will be set.

NOTE : The flag will be reset at the end of the V-BLANK period.

ADDRESS : 213FH
NAME : *STAT78
CONTENTS : PPU STATUS FLAG & VERSION NUMBER



DISPLAY METHOD
- 0 : NTSC
- 1 : PAL

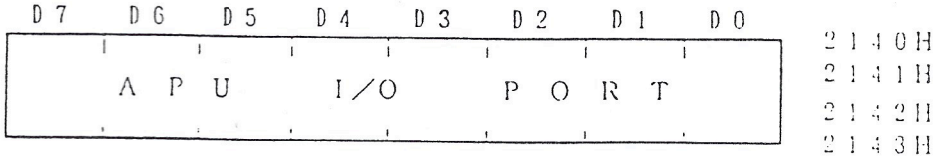
EXTERNAL LATCH FLAG : When the external signal (Light Pen. etc.) is applied. it enables to latch the H/V counter value.

FIELD : This is a status flag. which indicates whether 1st field is scanned or 2nd field is scanned the interlace mode. (The definition is different from the field of NTSC)
- 0 : 1ST FIELD
- 1 : 2ND FIELD

- When this register is read. registers <213CH> <213DH> will be initialized individually in the order of Low and High.

~~SR~~
LDA AD 3F 21
LDA.L AF 3F 21 00
LDX AE 3F 21
LDY AC 3F 21
} A9 10 EA [EA]

ADDRESS : 2140H / 2141H / 2142H / 2143H
NAME : APUIO0 / APUIO1 / APUIO2 / APUIO3
CONTENTS : COMMUNICATION PORT WITH APU



- This port provides more registers for the purpose of IN/OUT. which are 8 registers in total in the APU.
  Therehore. the different register will be accessed. whether reading or writing for the same address.

- See APU MANUAL for the details of the communication method

SUPER FAMICOM

REGISTER (PPU)

* * * * APPENDIN * * * *

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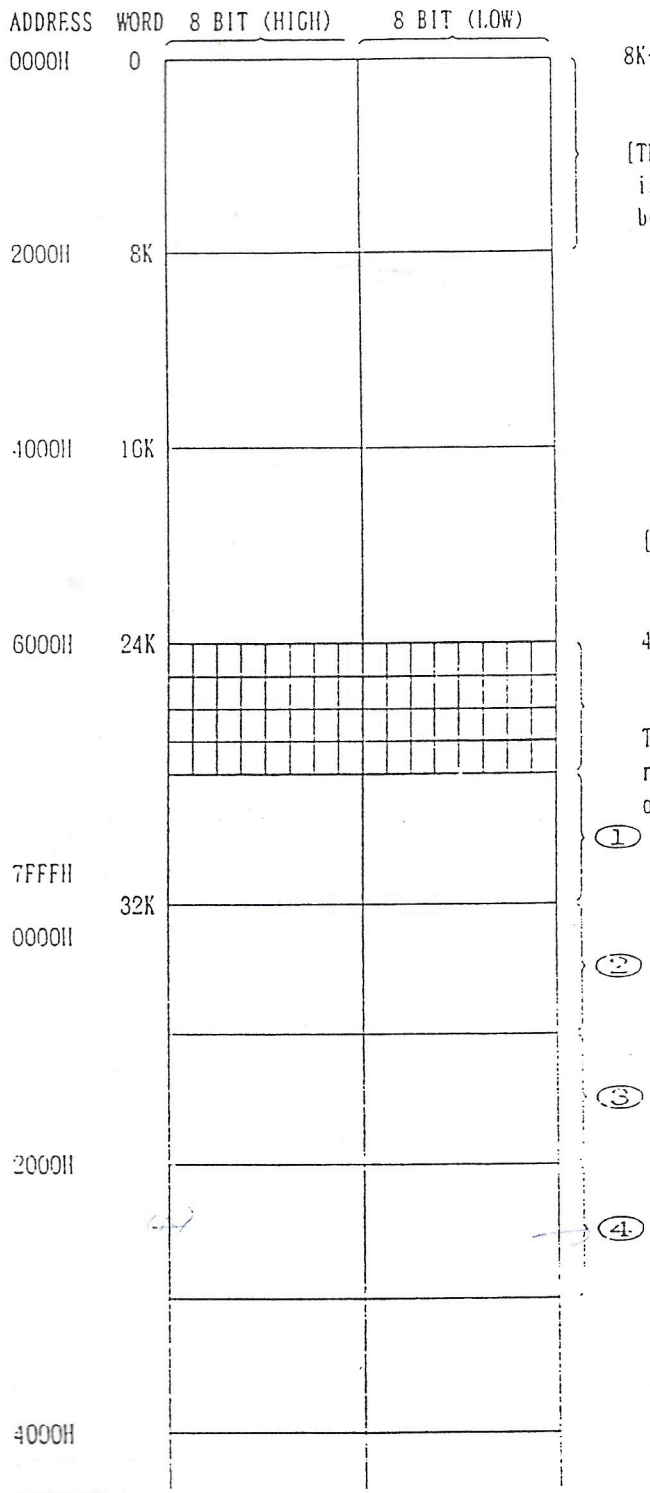
V — RAM



8K-WORD : This is a area which is designated by "OBJ NAME BASE ADDRESS" of the register <2101H>.
(32K-WORD / 4-Partition)
[The BA2 of the register <2101H> "OBJ NAME BASE ADDRESS is used for expansion purpose. and it will normally be ignored.]

[In case BA1=1 and BA0=1 are set by "OBJ NAME BASE ADDRESS"]

4K-WORD :This is a lower 4K-WORD of the area (8K-WORD) designated by "OBJ NAME BASE ADDRESS" of the register <2101H>.
The combination of this 4K-WORD and the 4K-WORD remaining will be determined by "OBJ NAME BASE SELECT" of the register <2101H>.

OBJ Name Select

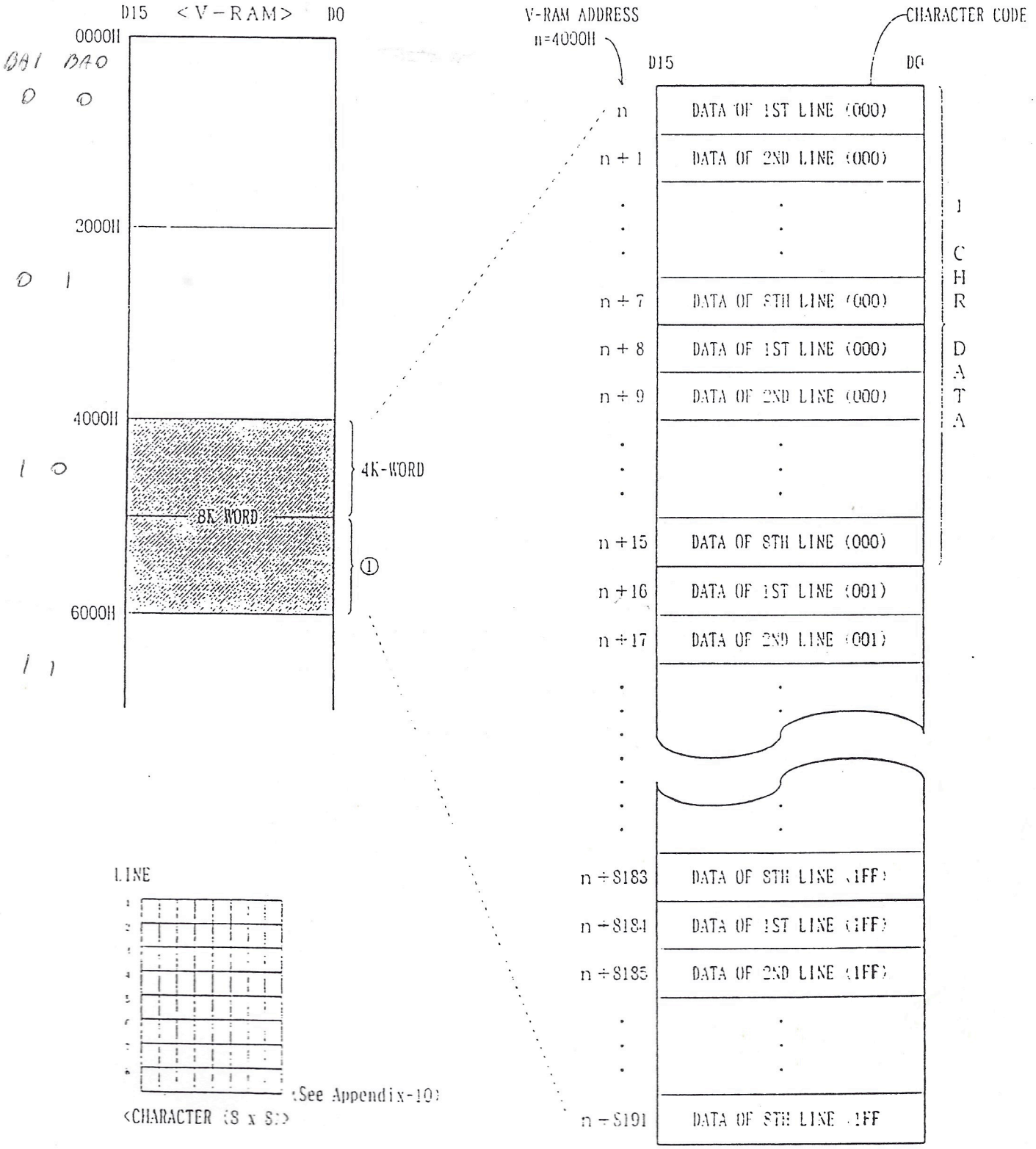
N1	N0	COMBINATION
0	0	4K-WORD - ①
0	1	4K-WORD - ②
1	0	4K-WORD - ③
1	1	4K-WORD - ④

OBJECT DATA TO BE STORED

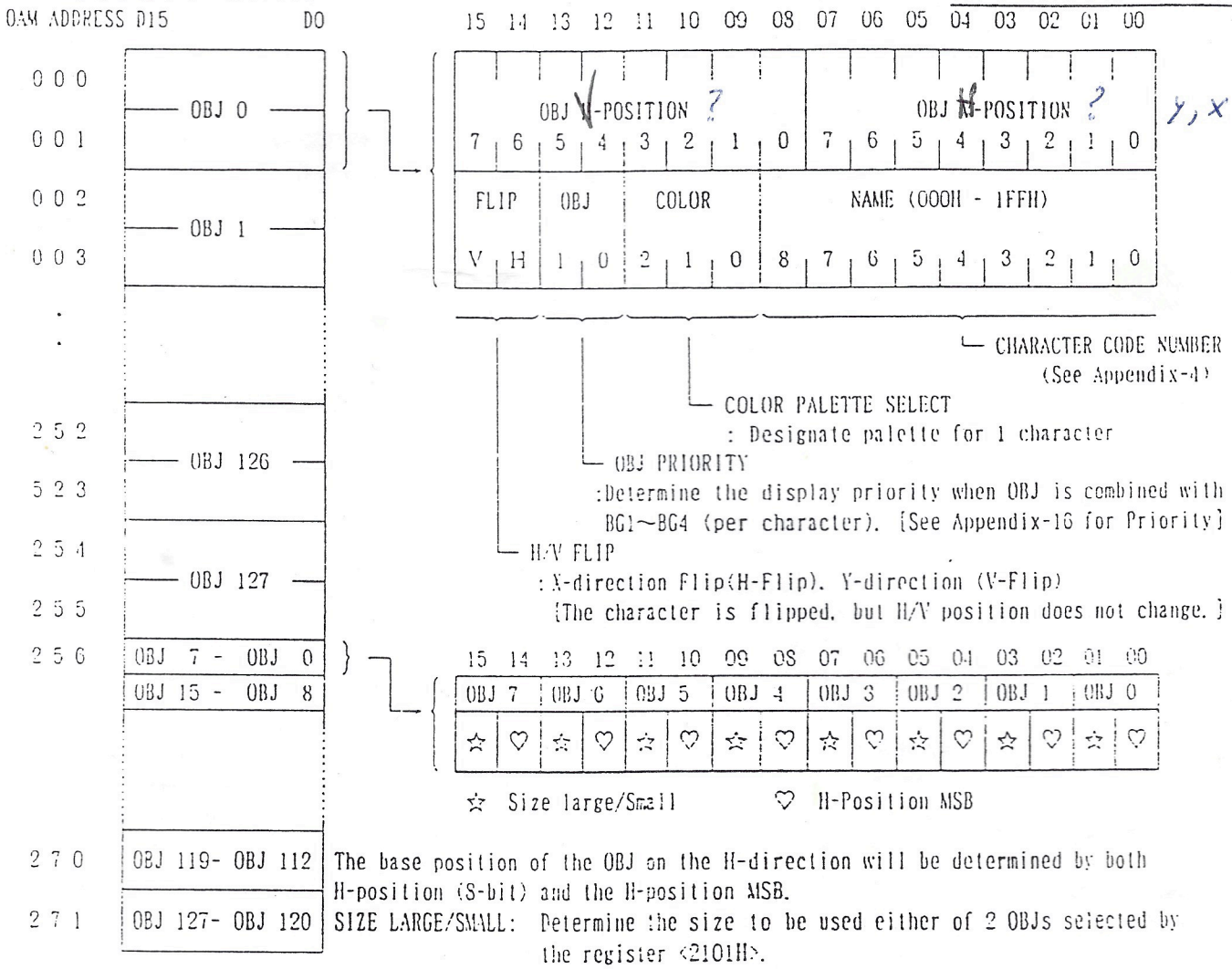
4 BIT CONSTRUCTION [8 x 8 x 4 Bit (16 WORD)/Character] (See Appendix-10)

8 x 8 (Character Size) x 4 (Bit Construction) x 512 (Number of character) ——— 16K-BYTE

[In case BA1=1 and BA0=0 are set by "OBJ NAME BASE ADDRESS" and also N1=0 and N0=0 are set by "OBJ NAME SELECT"]



OBJECT DATA

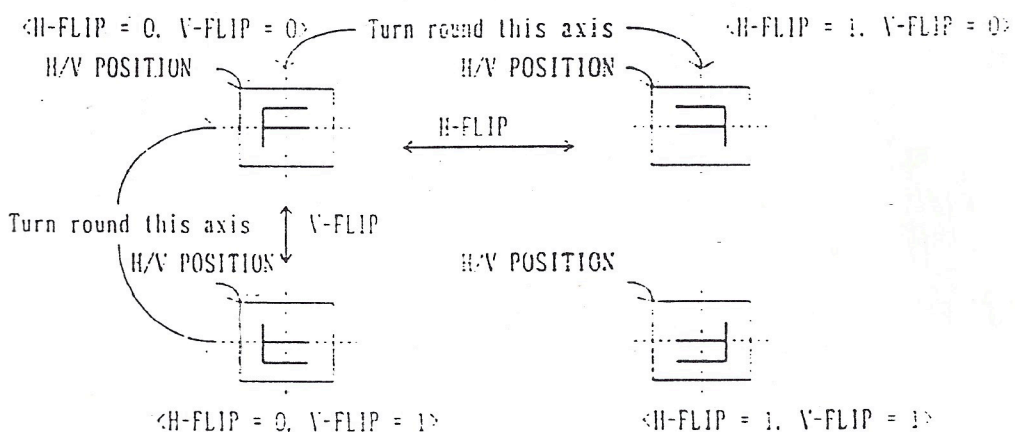

OAM ADDRESS D15 D0
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
000
001
OBJ 0
OBJ V-POSITION ?
OBJ H-POSITION ?
y, x
7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0
002
003
OBJ 1
FLIP OBJ COLOR NAME (000H - 1FFH)
V H 1 0 2 1 0 8 7 6 5 4 3 2 1 0
CHARACTER CODE NUMBER
(See Appendix-4)
COLOR PALETTE SELECT
: Designate palette for 1 character
OBJ PRIORITY
:Determine the display priority when OBJ is combined with
BG1~BG4 (per character). [See Appendix-16 for Priority]
H/V FLIP
: X-direction Flip(H-Flip), Y-direction (V-Flip)
[The character is flipped, but H/V position does not change.]
252
OBJ 126
523
254
OBJ 127
255
256
OBJ 7 - OBJ 0
OBJ 15 - OBJ 8
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
OBJ 7 OBJ 6 OBJ 5 OBJ 4 OBJ 3 OBJ 2 OBJ 1 OBJ 0
☆ ♡ ☆ ♡ ☆ ♡ ☆ ♡ ☆ ♡ ☆ ♡ ☆ ♡ ☆ ♡
☆ Size large/Small
♡ H-Position MSB
270
OBJ 119- OBJ 112
271
OBJ 127- OBJ 120

The base position of the OBJ on the H-direction will be determined by both H-position (8-bit) and the H-position MSB.

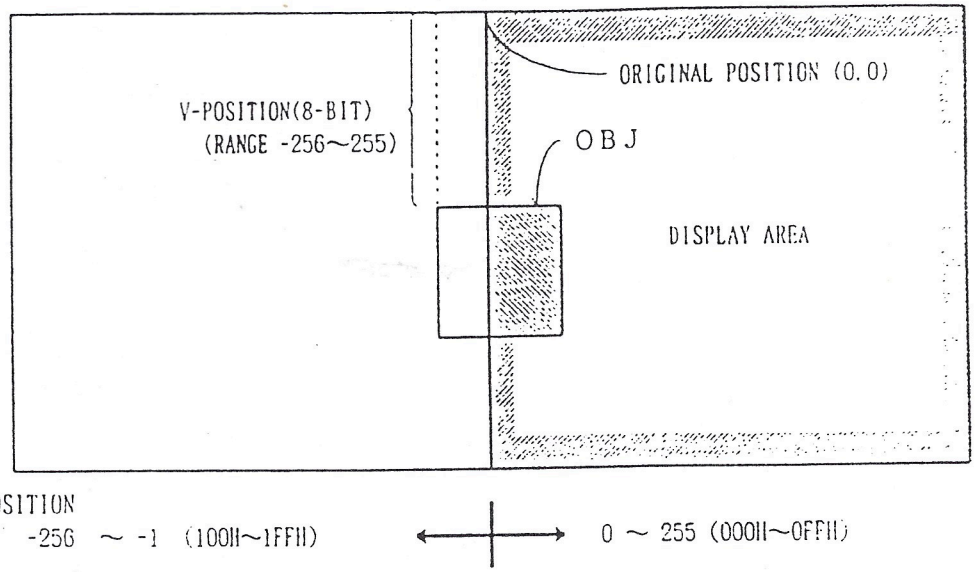
SIZE LARGE/SMALL: Determine the size to be used either of 2 OBJs selected by the register <2101H>.

- 0 : Select small size
- 1 : Select large size

H/V FLIP

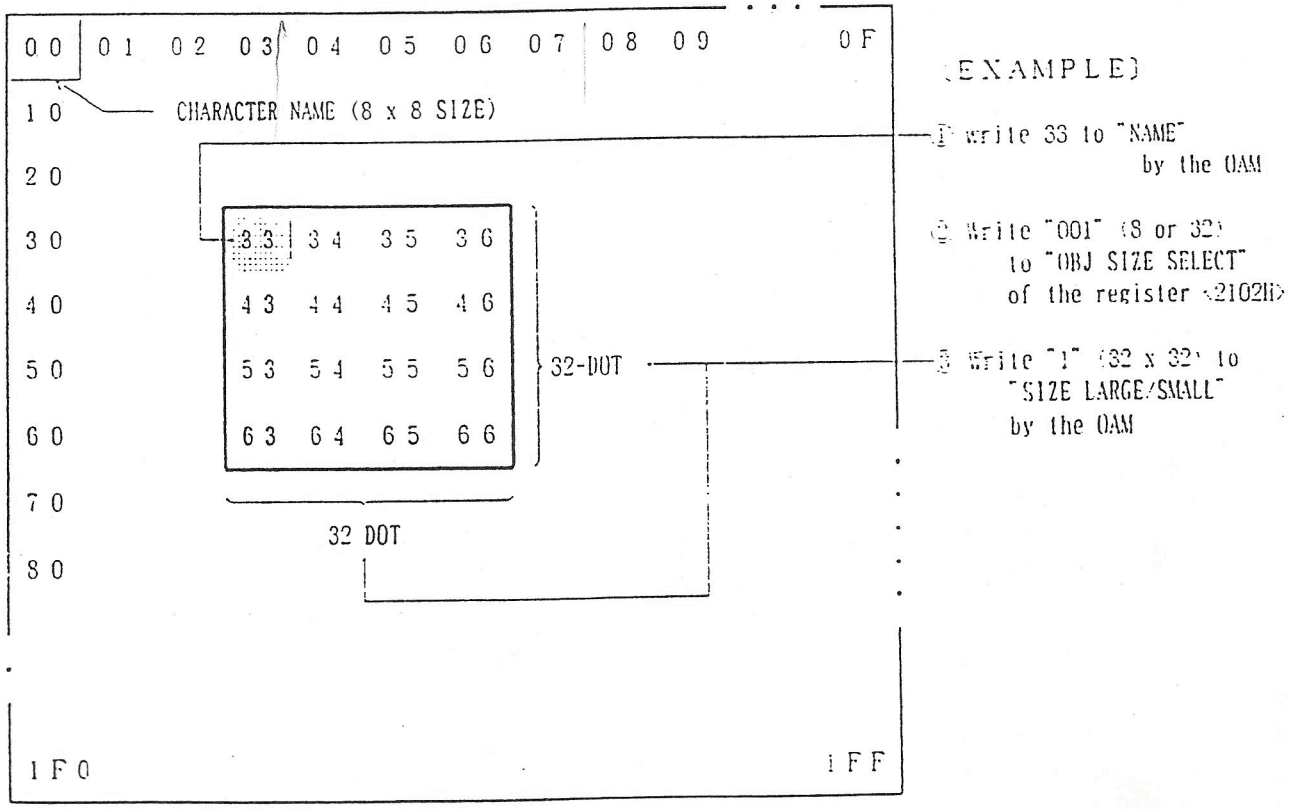


OBJECT DISPLAY



(NOTE-1) The H-position is a complementary expression of 2 (9-bit).
(NOTE-2) The coordinate of the OBJ displayed is shifted down compared to the coordinate of the BG displayed. {Interlace : 2-dot / Non-Interlace : 1-dot} (See Appendix-8)
(NOTE-3) "001H" is basically prohibited to use for 9-bit of the H-Position. (If it is used, it must be counted as OBJ quantity displayed even it is not displayed on the screen.)

OBJECT CHARACTER DATA CONSTRUCTION (V-RAM)



In case the character code is 000 through 0FF, the V-RAM address per character data (8-word) will be "n(Name Base Address) + N(name) x 16 ~ n + N x 16 + 15". And in case the character code is 100 through 1FF, it will be "n + Ns (Name Select) x 4K + N x 16 ~n + Ns x 4K + N x 16 + 15"

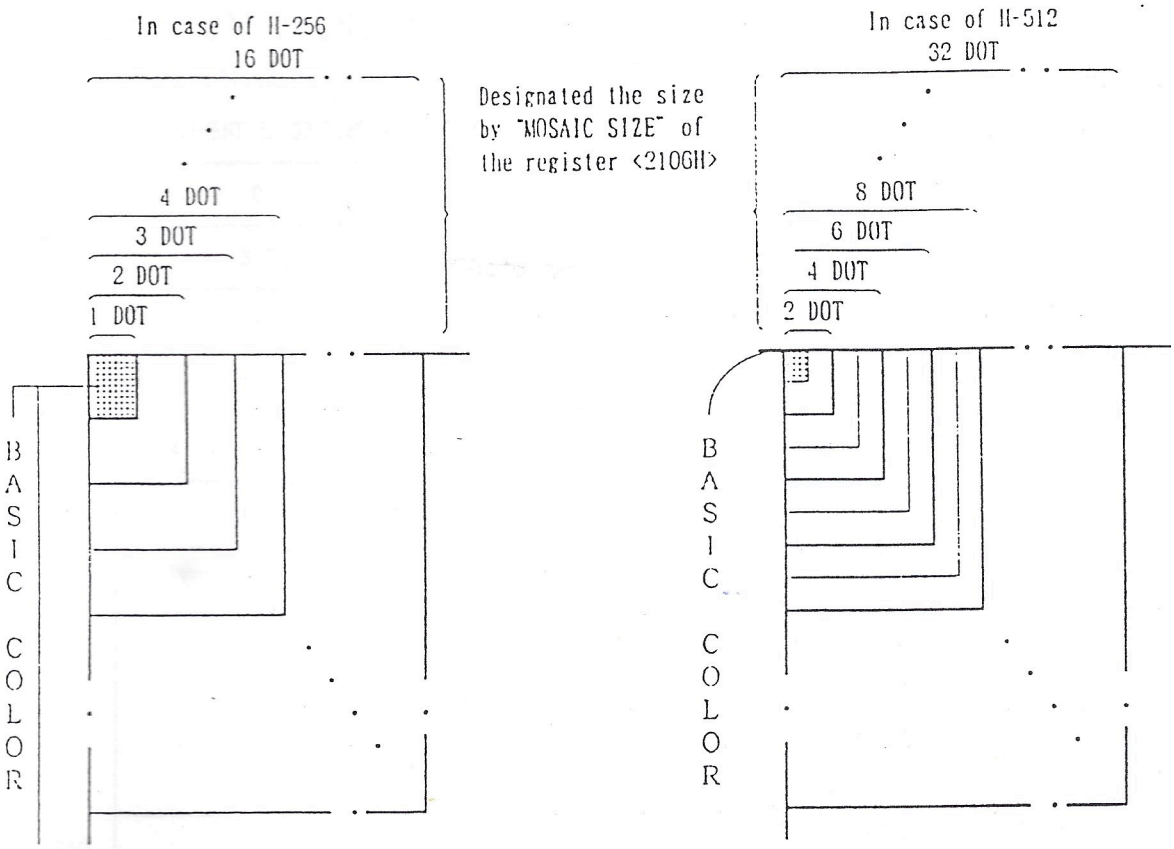
OBJECT MODE

# OF CELLS DISPLAYED	128			
CELL SIZE	8×8	16×16	32×32	64×64
# OF LINES DISPLAYED	32-pcs (converted to 8x8 size)			
# OF CELL-COLOR	16			
# OF PALETTE	8			
# OF COLOR ON SCREEN	128			
ATTRIBUTE	H-FLIP, V-FLIP FUNCTION DISPLAY PRIORITY (Select priority against BG)			

BG MODE

MODE	# OF SCREEN DISPLAYED	SCREEN	# OF CELL DOT	# OF CELL COLOR	# OF PALETTES	# OF COLORS PER SCREEN	FUNCTION
0	MAX 4	BG 1	8×8 & 16×16	4	8	32	H/V SCROLL H-FLIP, V-FLIP WINDOW MOSAIC FIXED-COLOR ADDITION SCREEN COLOR ADDITION
		BG 2		4	8	32	
		BG 3		4	8	32	
		BG 4		4	8	32	
1	MAX 3	BG 1		16	8	128	
		BG 2		16	8	128	
		BG 3		4	8	32	
2	MAX 2	BG 1		16	8	128	① ① Offset value can be set in H/V direction against the cell
		BG 2		16	8	128	
3	MAX 2	BG 1		256	1	256	
		BG 2		16	8	128	
4	MAX 2	BG 1		256	1	256	① ② H-512 mode vertical expansion caused interlace
		BG 2		4	8	32	
5	MAX 2	BG 1		16	8	128	② ③ Enlargement Reduction Rotation
		BG 2		4	8	32	
6	1	BG 1		16	8	128	①②
7	1	BG 1	8×8	256	1	256	③

MOSAIC SCREEN

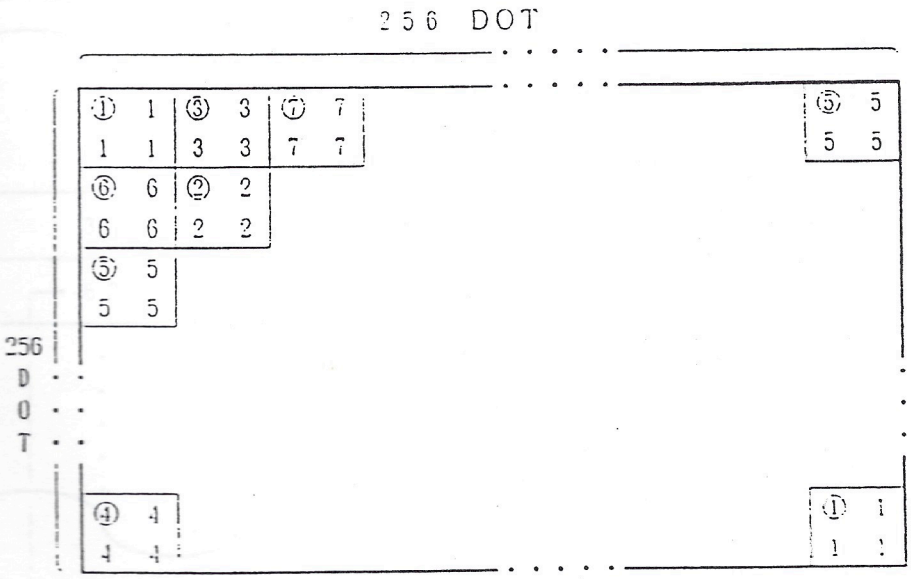


*all dots of the size designated become this color.

In case of the H-Pseudo 512 mode. 2 x 2-dot mosaic can be made in size-0. (See No.3)

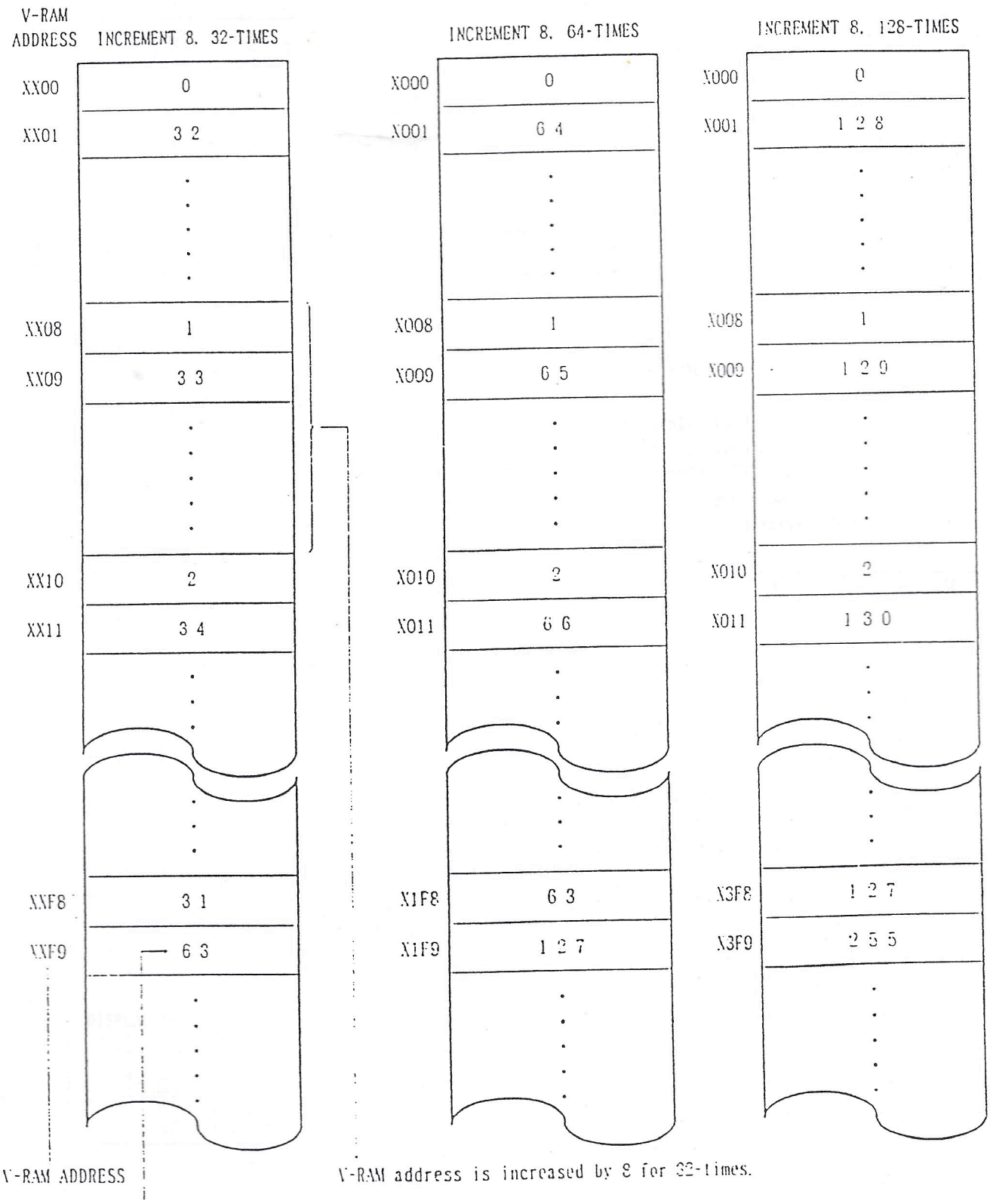
MOSAIC SCREEN DISPLAY EXAMPLE (BG SCREEN)

(When the mosaic size is 2x2-dot in the 256-mode)



○ is the basic color data

ADDRESS INCREMENT VALUE SET (THE ORDER OF ACCESSING)



ORDER OF ACCESS (corresponding to the address designated by the register (210H)~211H))

BG SC DATA (MODE 0~6)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
FLIP V	FLIP H	BG Pri.	COLOR 2	COLOR 1	COLOR 0	NAME 9	NAME 8	NAME 7	NAME 6	NAME 5	NAME 4	NAME 3	NAME 2	NAME 1	NAME 0

(000H~3FFH)

CHARACTER CODE NUMBER

COLOR PALETTE SELECT : PALETTE DESIGNATION PER CHARACTER <8-Palettes>

BG PRIORITY : Determine the display priority per character in case OBJ and BG1 ~BG4 are combined on the same screen.

H/V FLIP : X-Directional Flip (H-FLIP), Y-Directional Flip (V-FLIP)

BG SCREEN H/V SCROLL

REGISTER <210DH><210FH>
<2111H><2113H>

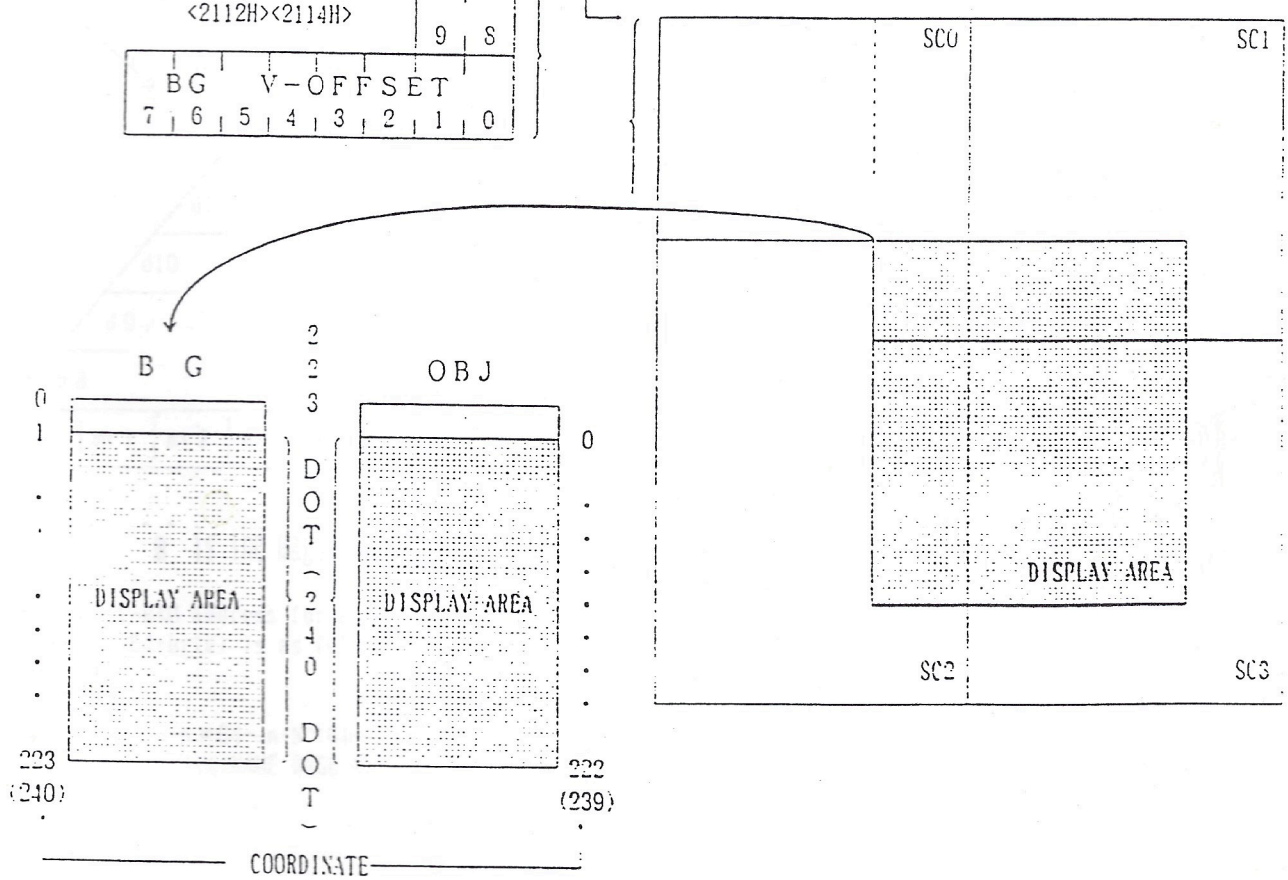
9	8	7	6	5	4	3	2	1	0
BG H-OFFSET									

REGISTER <210EH><2110H>
<2112H><2114H>

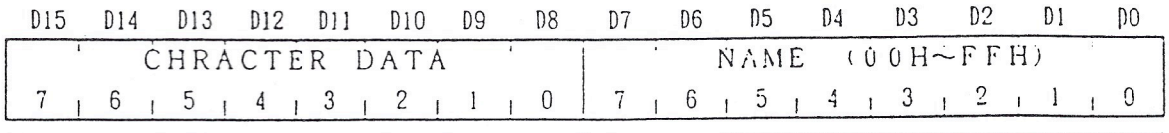
9	8	7	6	5	4	3	2	1	0
BG V-OFFSET									

- RANGE OF H-SCROLL
  0 ~ 1024 DOT
- RANGE OF V-SCROLL
  0 ~ 1024 DOT

H/V scroll range may be changed and 2-dot scroll may be possible, depending on the combination of the modes (512, 16-size, interlace etc.).
Also, SC size may be changed against the screen. (See Appendix-18 & 19)

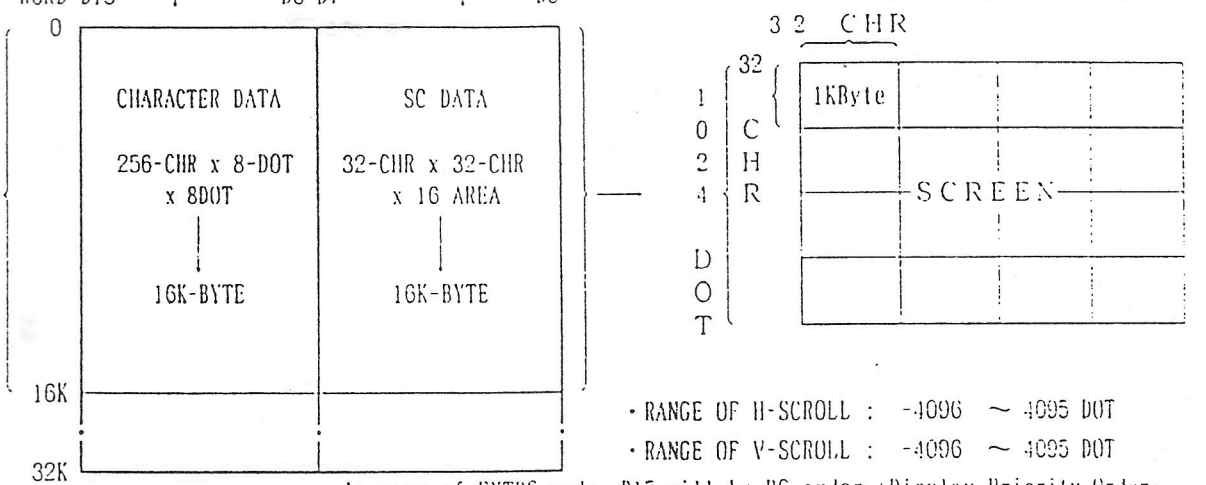


BG SC DATA (MODE 7)



<V-RAM>

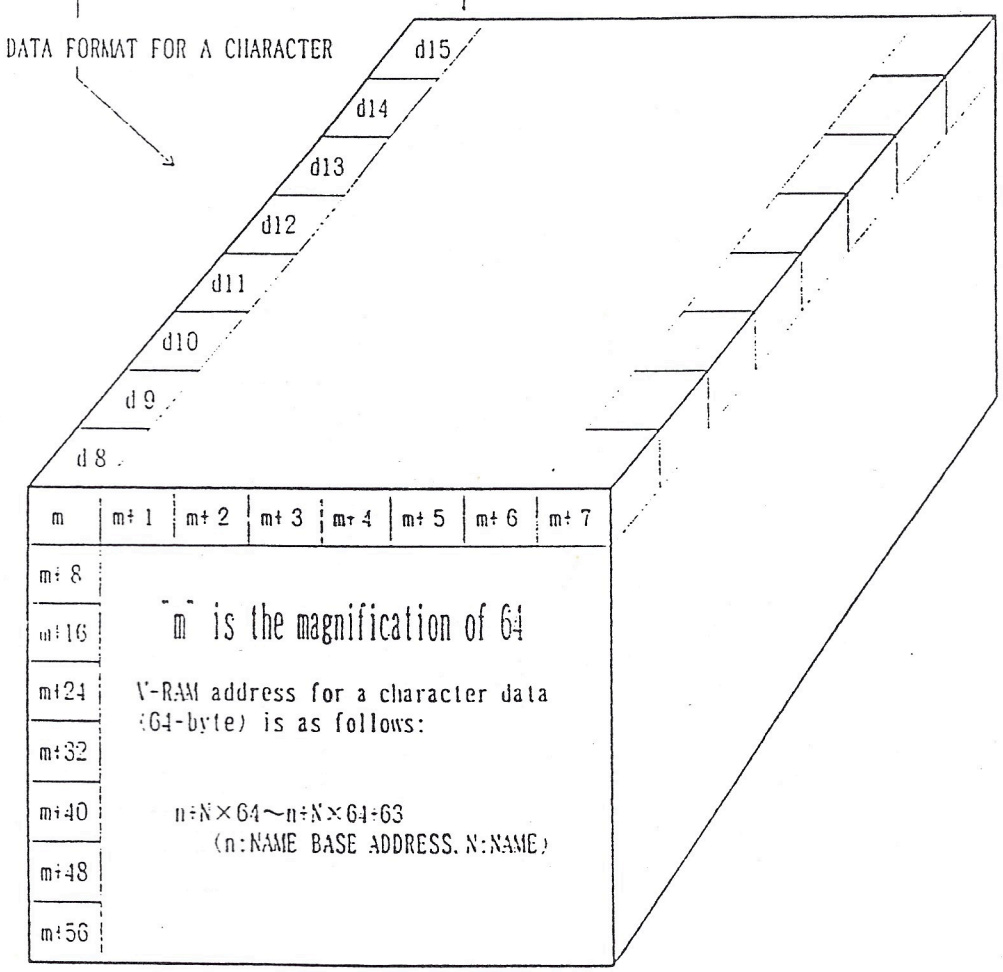
32-CHR x 4-SCREEN x 8-DOT/CHR = 1024-DOT



- RANGE OF H-SCROLL : -4096 ~ 4095 DOT
- RANGE OF V-SCROLL : -4096 ~ 4095 DOT

In case of EXTBG mode. D15 will be BG order (Display Priority Order).

DATA FORMAT FOR A CHARACTER



"m" is the magnification of 64

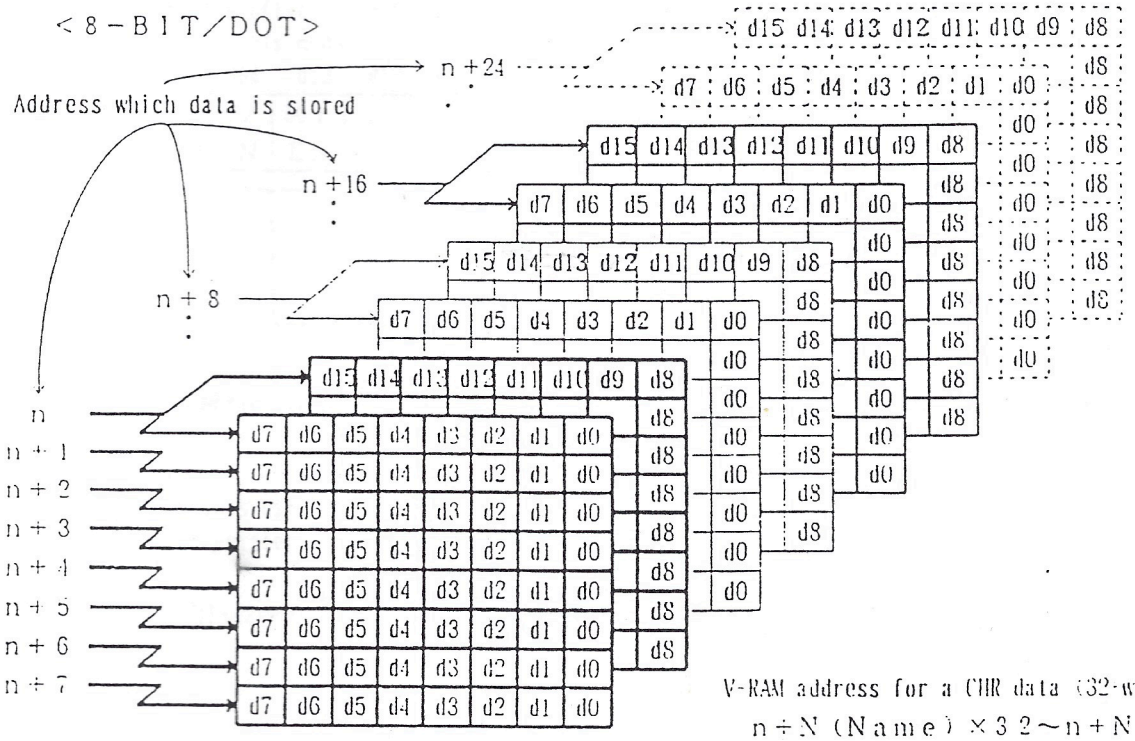
V-RAM address for a character data (64-byte) is as follows:

n=N×64~n=N×64+63
(n:NAME BASE ADDRESS, N:NAME)

CHR DATA CONSTRUCTION

※ n : Name Base Address

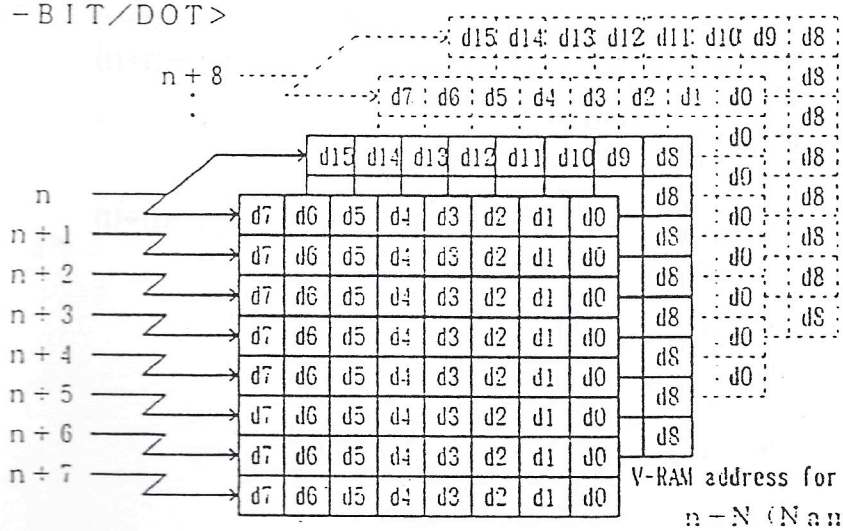
<8-BIT/DOT>



V-RAM address for a CHR data (32-word) is as follows:

n+N (Name) ×32～n+N×32+31

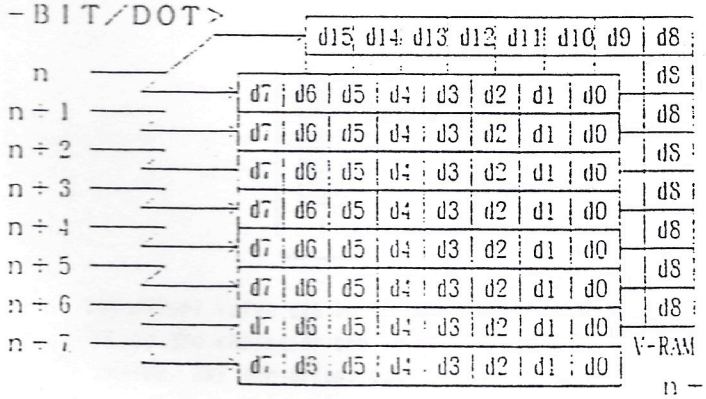
<4-BIT/DOT>



V-RAM address for a CHR data (16-word) is as follows:

n-N (Name) ×16～n-N×16+15

<2-BIT/DOT>



V-RAM address for a CHR data (8-word) is as follows:

n-N (Name) ×8～n-N×8-7

OFFSET CHANGE MODE

The offset change mode can be used in the BG mode 2, 4 and 6, and the following data is required in this mode.

d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0
H/V	BG2 EN	BG1 EN				OFFSET DATA									

H,V OFFSET VALUE (in the change mode)

In case of the H-OFFSET, the data (D0 ~D2) will be invalid.
In case of the character (16 x 16), "D3" is effective every 3rd.

OFFSET MODE ENABLE
- 0 : Disable
- 1 : Enable

Designate either H-OFFSET or V-OFFSET for the OFFSET data d0 ~d9. (Only BG MODE 4 is effective)
- 0 : H-OFFSET
- 1 : V-OFFSET

This data should be written to the address, which is designated by "BG3 SC BASE ADDRESS" of register <2109H>, using the mode designated. (See below)

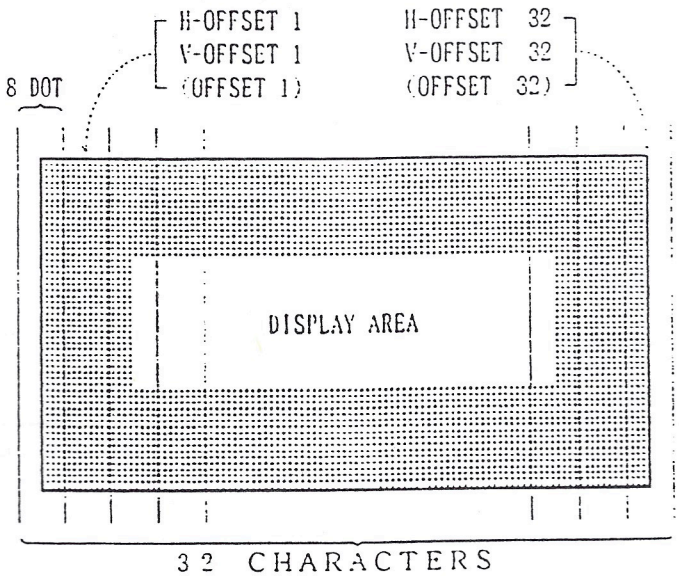
<MODE 2, 6>

(1)+(2)+ 0	H-OFFSET 1
	. . .
(1)+(2)+1F	H- OFFSET 32
(1)+(2)+20	V- OFFSET 1
	. . .
(1)+(2)+3F	V- OFFSET 32

<MODE 4>

(1)+(2)+ 0	OFFSET 1
(1)+(2)+ 1	OFFSET 2
	. . .
(1)+(2)+1F	OFFSET 32

In case BG3 SC size is S1=0, S0=0
- (1) : BG3 SC Base Address ({value set by "d2"~"d7" of <2109H>}×1024)
- (2) : BG3 SC Offset Address ({value set by "d3"~"d7" of <2112H>}×32 + {value set by "d3"~"d7" of <2111H>})

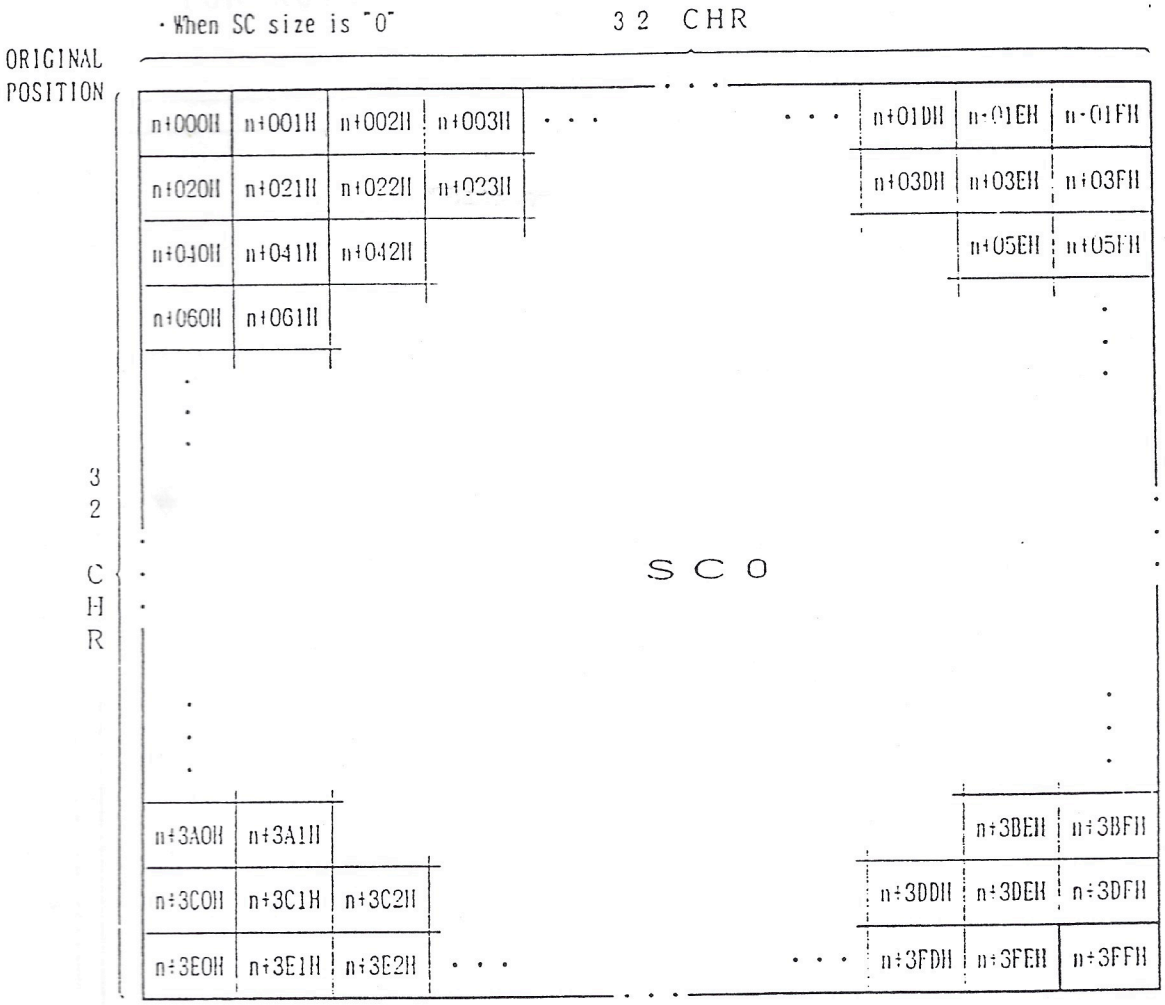


The offset value can be changed by each column (character unit).
Up to 3rd character can be seen horizontally on the screen by setting the offset value of the entire screen, but the offset can not be changed for 1st character (0 character).

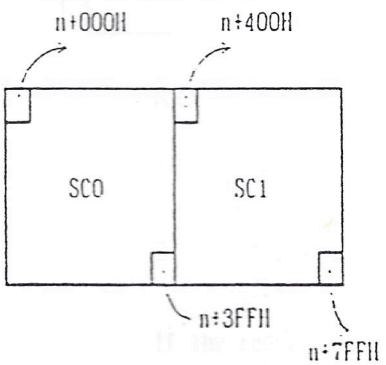
BG SCREEN

(n=SC Base Address(6-BIT)× 400H)

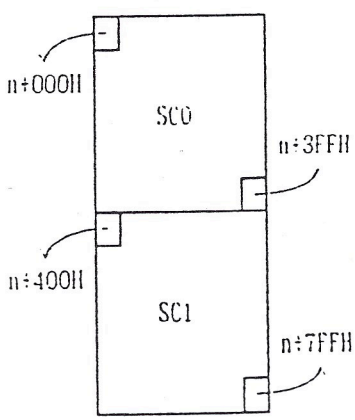
・When SC size is "0"



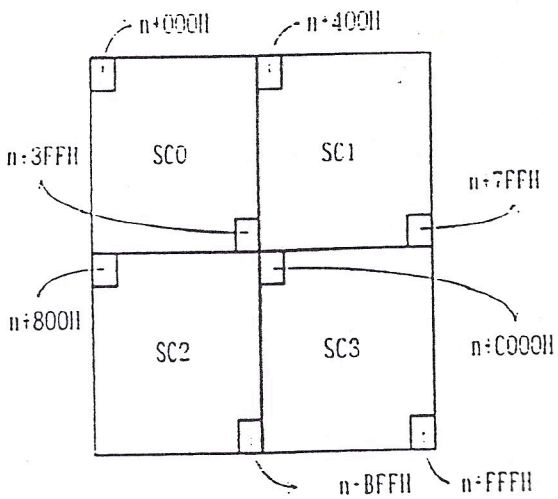
・When SC size is "1"



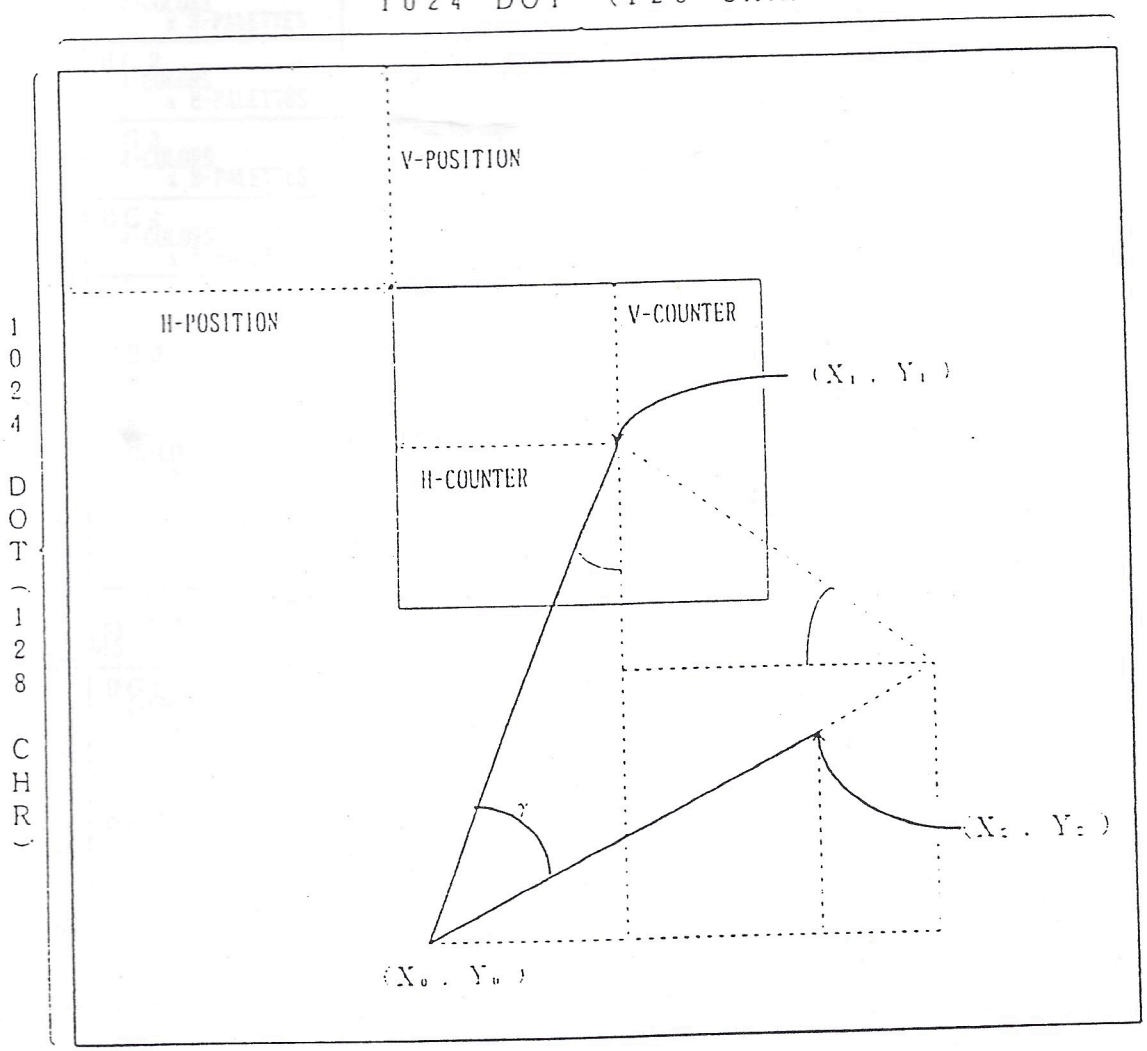
・When SC size is "2"



・When SC size is "3"



OPERATION (ROTATION/ENLARGEMENT/REDUCTION)



ROTATIONAL TRANSFORM FORMULA

$$\begin{pmatrix} X_2 \\ Y_2 \end{pmatrix} = \begin{pmatrix} \cos\gamma & \sin\gamma \\ -\sin\gamma & \cos\gamma \end{pmatrix} \begin{pmatrix} X_1 - X_0 \\ Y_1 - Y_0 \end{pmatrix} + \begin{pmatrix} X_0 \\ Y_0 \end{pmatrix}$$

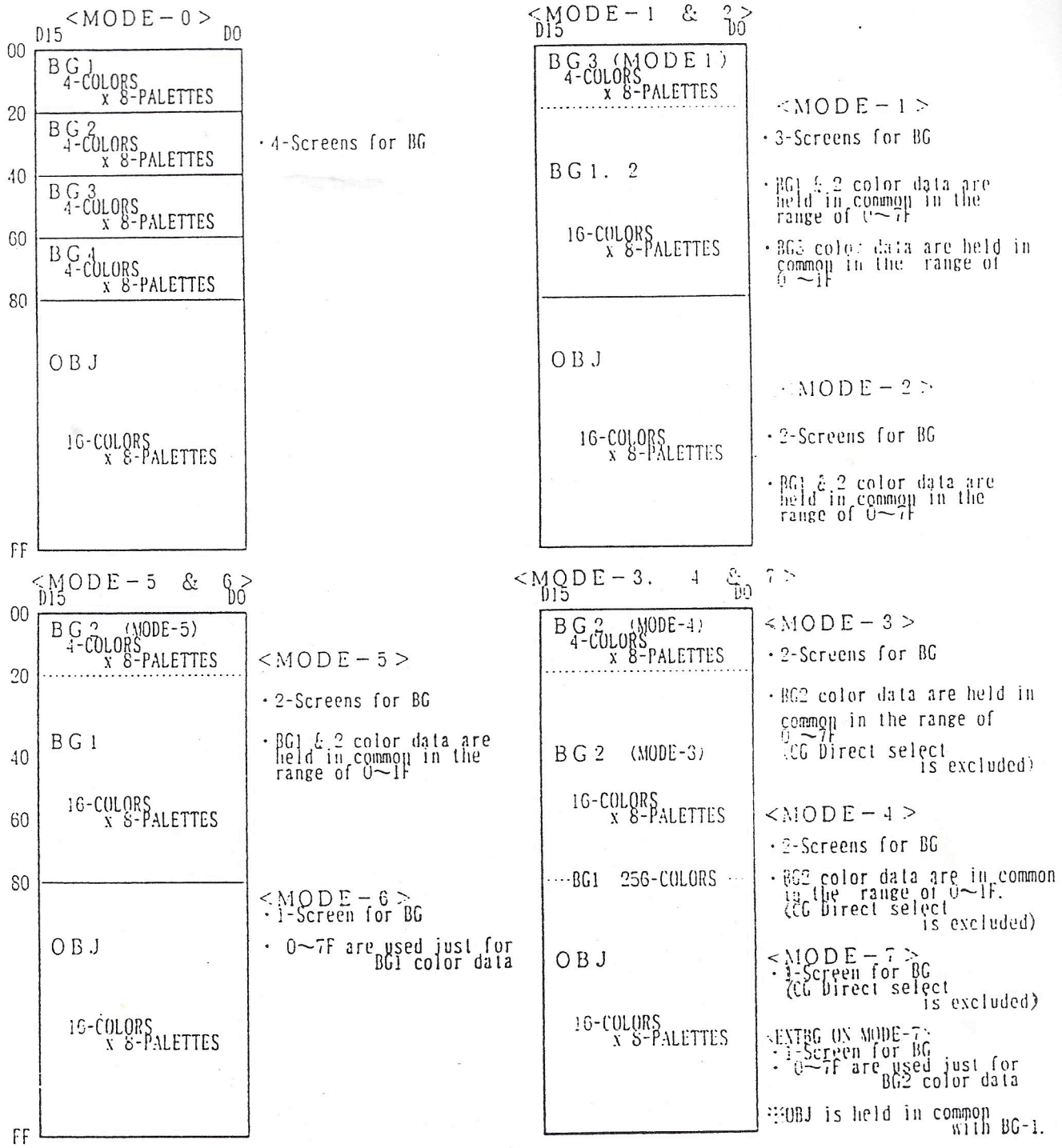
$X_0 \cdot Y_0$: Center Coordinate
$X_1 \cdot Y_1$: Display Coordinate
$X_2 \cdot Y_2$: Coordinate before calculation of display coordinate

If the reduction rates for X-dir (α) and the reduction rates for Y-dir (β) are considered, the formula described above will be as follows :

$$\begin{pmatrix} X_2 \\ Y_2 \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \begin{pmatrix} X_1 - X_0 \\ Y_1 - Y_0 \end{pmatrix} + \begin{pmatrix} X_0 \\ Y_0 \end{pmatrix}$$

$A = \cos\gamma \times (1/\alpha)$ $\quad B = \sin\gamma \times (1/\alpha)$
$C = -\sin\gamma \times (1/\beta)$ $\quad D = \cos\gamma \times (1/\beta)$

CG-RAM



CG-RAM COLOR DATA

BLUE					GREEN					RED				
d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0

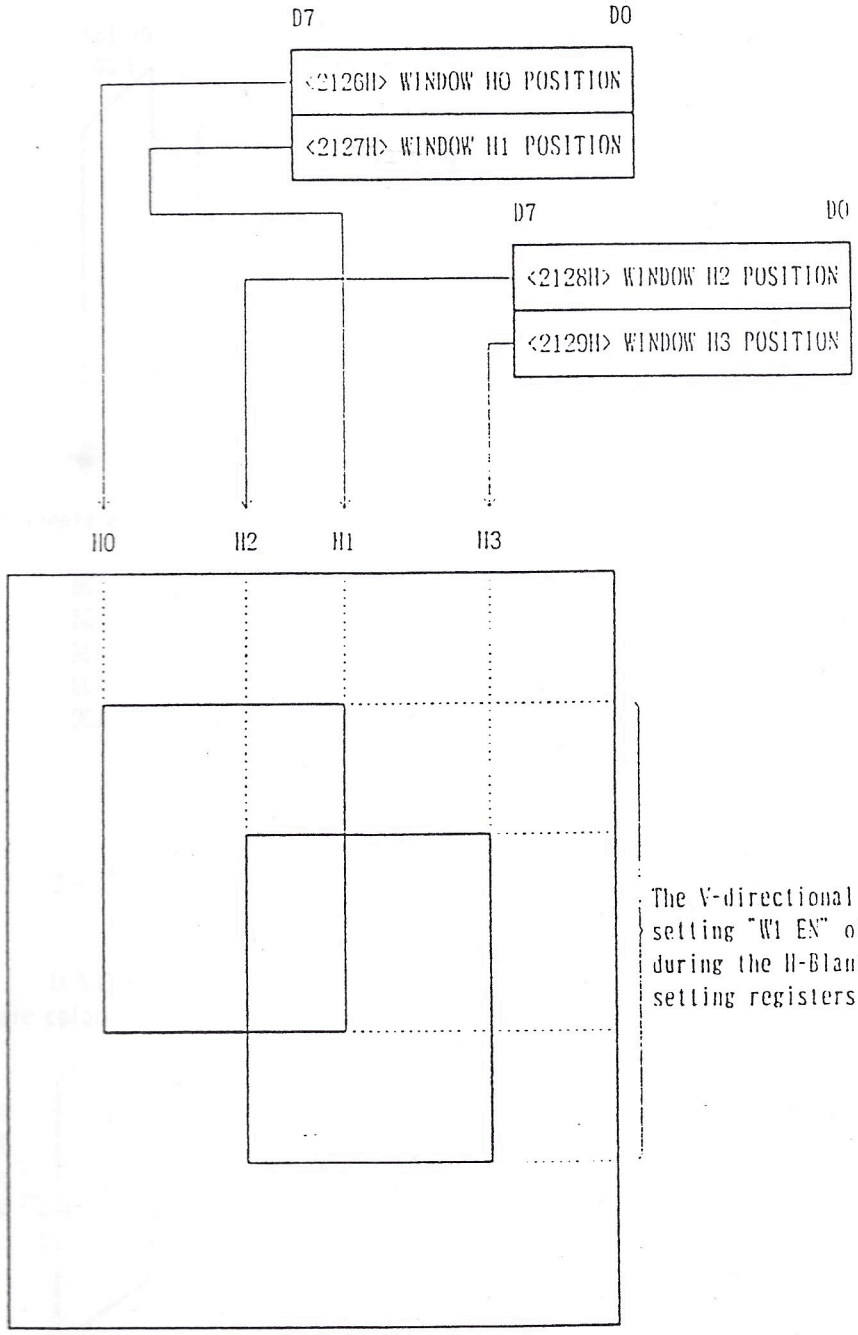
DIRECT SELECT COLOR DATA

BLUE					GREEN					RED				
DA7	DA6	CL2	0	0	DA5	DA4	DA3	CL1	0	DA2	DA1	DA0	CL0	0

NOTE : DA0~DA7 are used for the character dot data. CL0~CL2 are used for the BG-SC data of the color. However, in case of Mode-7, CL0 ~CL2 should be "0".
NOTE : If they are "0", it becomes transparent. The color of CG-RAM address "00H" will be background.

WINDOW

REGISTER<2126H>~<2129H>

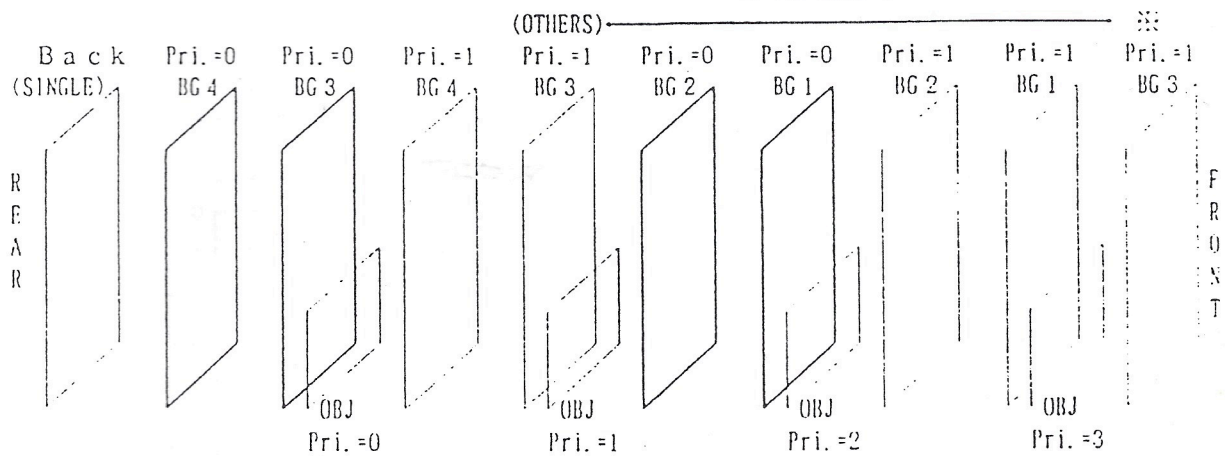


The V-directional position is determined by setting "W1 EN" of registers <2123H><2124><2125H> during the H-Blank period or determined by setting registers <2126H> ~<2129H>.

BG & OBJ PRIORITY

4-SCREEN/3-SCREEN MODE

※ In case "D3=1" is selected by register <2105H> in the mode-1



<Example of Display Priority (in case of mode 0 & 4)>

BG1 Pri.=0
BG2 Pri.=1
BG3 Pri.=0
BG4 Pri.=1
OBJ Pri.=2

are set

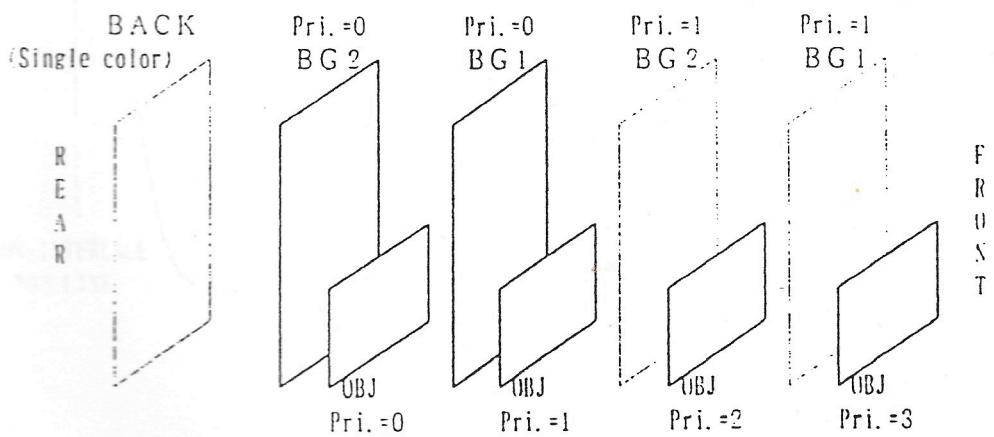
High Priority (FRONT) ——— Low Priority (REAR)

BG2-OBJ-BG1-BG4-BG3-Back

(Displayed in the order of above)

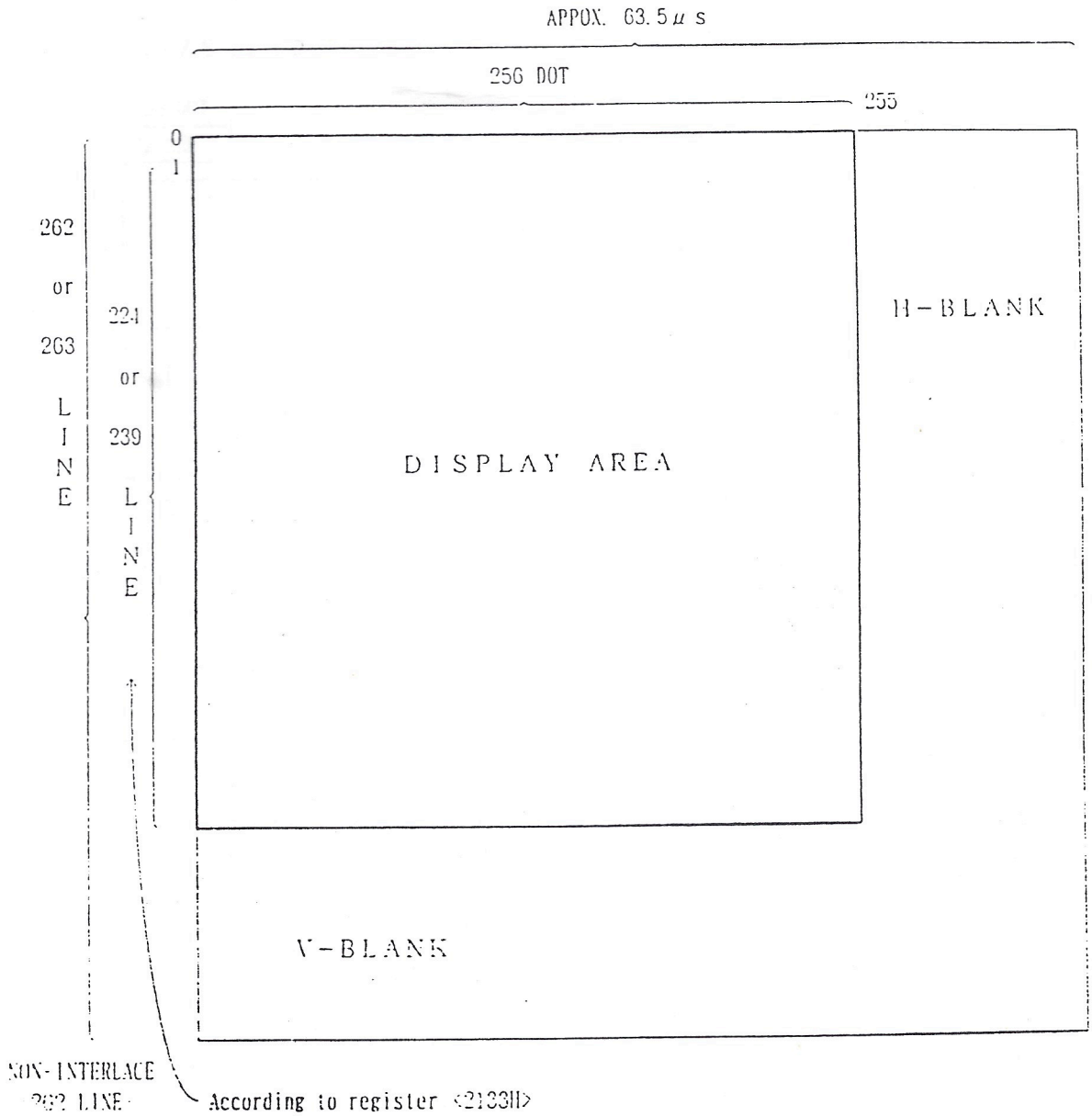
2-SCREEN/1-SCREEN MODE

(in case Mode 2~7 is selected by the register <2105H>)



NOTE : In case of the display priority between the OBJs, normally the lower numbered OBJ will be displayed as higher priority. <See Page-35 for exception>
This display priority will be determined before the priority between OBJ and BG is determined.

SCREEN

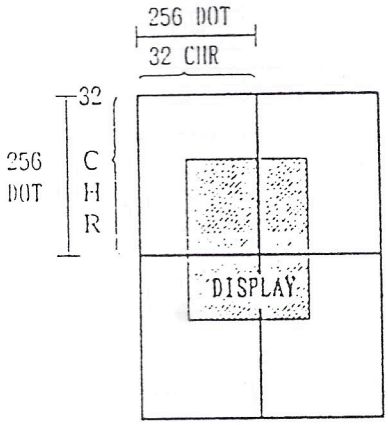

APPOX. 63.5μs
256 DOT
255
0
1
262
or
263
LINE
224
or
239
LINE
H-BLANK
DISPLAY AREA
V-BLANK
NON-INTERLACE
262 LINE
According to register <2133H>

BG SCREEN

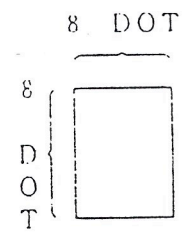
H/V SCROLL ① (Scroll range by the combination of modes. and SC size against screen)
<Example in case SC size is "3" (SEE NO.4)>

★In case of 0, 1, 2 & 4

・BG SIZE〔8x8〕

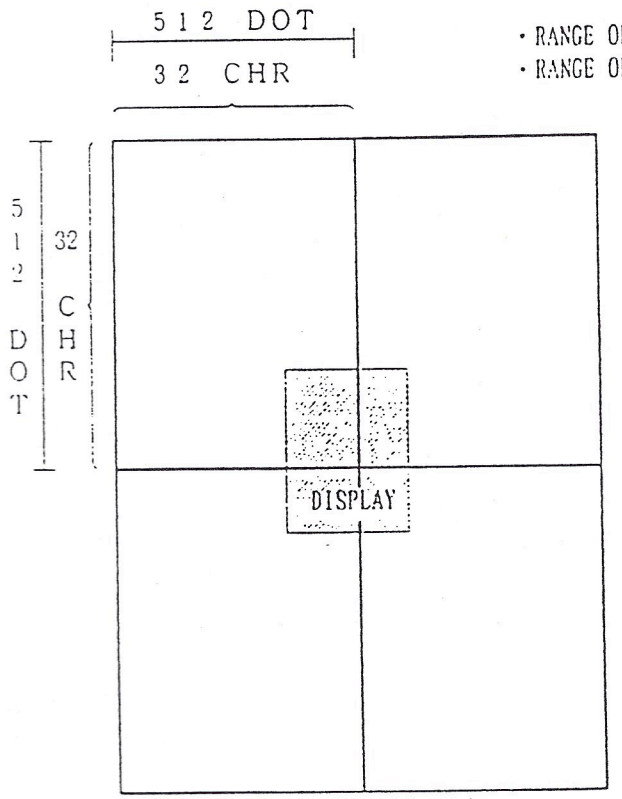


SC SCREEN

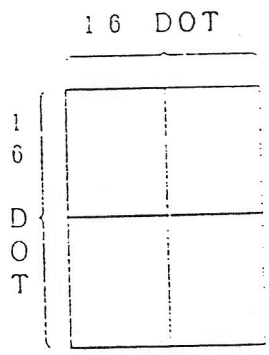


・RANGE OF H-SCROLL: 0～ 511 (Scroll 1-dot to the left by adding 1
・RANGE OF V-SCROLL: 0～ 511 (Scroll 1-dot to the up by adding 1

・BG SIZE〔16x16〕



・RANGE OF H-SCROLL: 0～ 1023 (Scroll 1-dot to the left by adding 1
・RANGE OF V-SCROLL: 0～ 1023 (Scroll 1-dot to the up by adding 1)

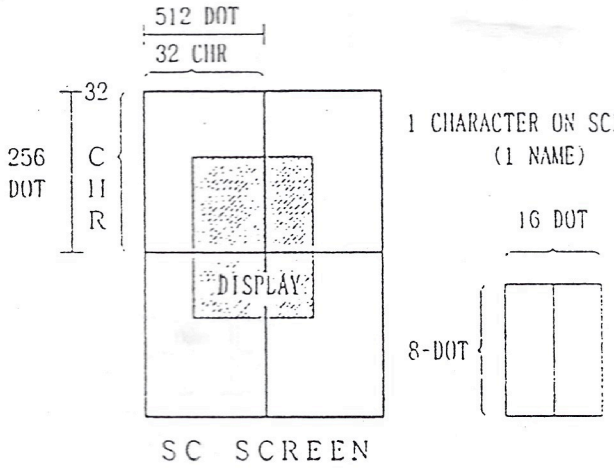


BG SCREEN

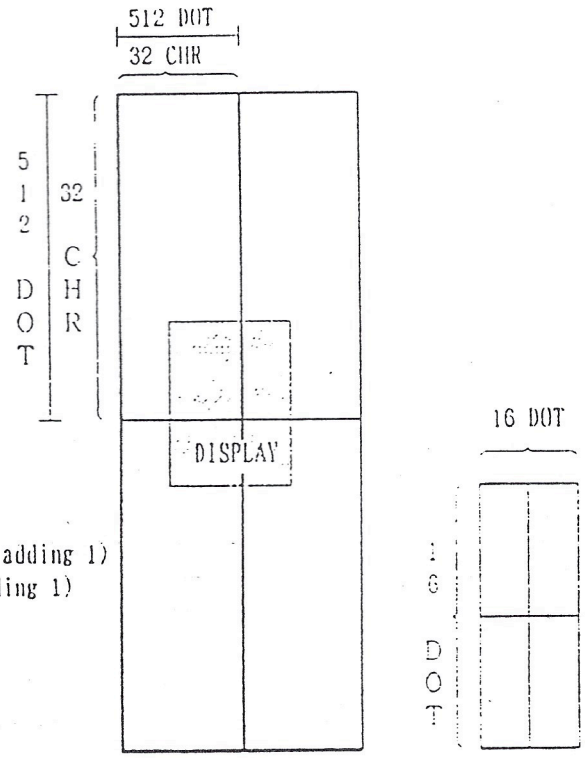
H/V SCROLL ② (Scroll range by the combination of modes, and SC size against screen)
<Example in case SC size is "3" (SEE NO.4)>

★IN CASE OF MODE-5, MODE-6 & NON-INTERLACE

・BG SIZE [8 x 8]



・BG SIZE [16 x 16]

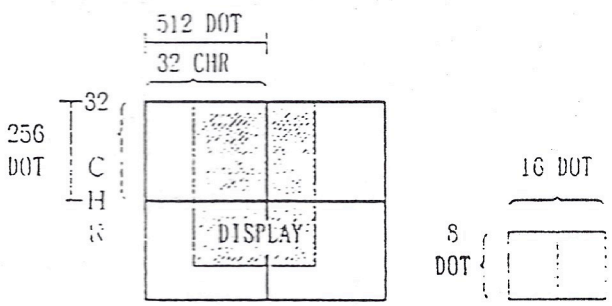


・RANGE OF H-SCROLL:0 ～ 511 (Scroll 2-dots to the left by adding 1)
・RANGE OF V-SCROLL:0 ～ 511 (Scroll 1-dot to the up by adding 1)

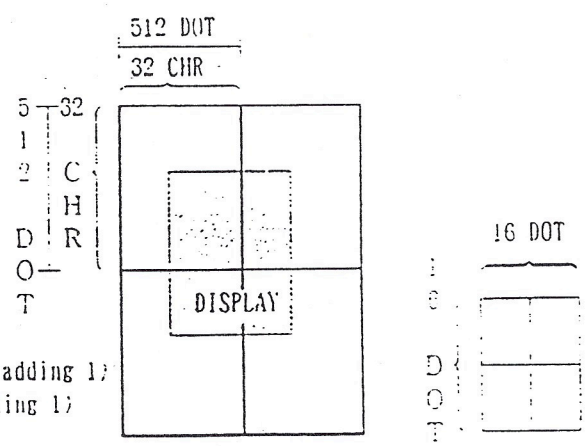
・RANGE OF H-SCROLL: 0～ 511 (Scroll 2-dots to the left by adding 1)
・RANGE OF V-SCROLL: 0～ 1023 (Scroll 1-dot to the up by adding 1)

★IN CASE OF MODE-5 & 6. INTERLACE

・BG SIZE [8 x 8]



・BG SIZE [16 x 16]



・RANGE OF H-SCROLL: 0～ 511 (Scroll 2-dots to the left by adding 1)
・RANGE OF V-SCROLL: 0～ 511 (Scroll 1-dot to the up by adding 1)

・RANGE OF H-SCROLL: 0～ 511 (Scroll 2-dots to the left by adding 1)
・RANGE OF V-SCROLL: 0～ 1023 (Scroll 1-dot to the up by adding 1)

SUPER FAMICOM

REGISTER (CPU)

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ADDRESS : 4200H
NAME : NMITIMEN
CONTENTS : ENABLE FLAG FOR V-BLANK. TIMER INTERRUPT & JOY CONTROLLER READ

D7	D6	D5	D4	D3	D2	D1	D0	
NMI Enable		TIMER ENABLE V-EN	H-EN				JOY-C ENABLE	4200H

JOY CONTROLLER ENABLE
- 0 : Disable Automatic reading of the Joy Controller
- 1 : Enable Automatic reading of the Joy Controller

※ Reading the data can be started at the beginning of V-Blank period. but it takes about for 3 or 4 scanning period until completion of reading.

TIMER ENABLE
- V-EN : V-COUNT TIMER ENABLE
- H-EN : H-COUNT TIMER ENABLE

H EN	V EN	FUNCTION
0	0	Disable BOTH H & V
0	1	Enable H only. IRQ is applied by H-count timer value designated.
1	0	Enable V only. IRQ is applied by V-count timer value designated.
1	1	Enable both H & V. IRQ is applied by both H and V count timer value designated.

NMI ENABLE : Enable NMI at the point when V-blank begins
(When power is turned on or the reset signal is applied. it will be "0".)
- 0 : NMI DISABLE
- 1 : NMI ENABLE

ADDRESS : 4201H
NAME : WRIO
CONTENTS : PROGRAMABLE I/O PORT (OUT-PORT)

D7	D6	D5	D4	D3	D2	D1	D0	
I/O PORT								4201H
D7	D6	D5	D4	D3	D2	D1	D0	

- This is a Programable I/O port (OUT-PORT). The written data will be output directly from the OUT-PORT.
- When this is used as a INPORT. "1" should be written to the particular bit which will be used as a IN-PORT. The input data can be read by register (4213H).

ADDRESS : 4202H / 4203H
NAME : WRMPYA / WRMPYB
CONTENTS : MULTIPLIER & MULTIPLICAND BY MULTIPLICATION

D7	D6	D5	D4	D3	D2	D1	D0	
MULTIPLICAND-A								4202H
A7	A6	A5	A4	A3	A2	A1	A0	
MULTIPLIER-B								4203H
B7	B6	B5	B4	B3	B2	B1	B0	

- This is a register, which can set a Multiplicand (A) and a multiplier (B) for Absolute Multiplication of "A (8-BIT) × B (8-BIT) = C (16-BIT)"
- A PRODUCT (C) can be read by registers <4216H><4217H>.
- Set in the order of (A) and (B). The operation will start as soon as (B) has been set, and it will be completed right after 8-machine cycle period.
- Once the data of the A-REGISTER is set, it will not be destoroyed until new data is set.

ADDRESS : 4204H / 4205H / 4206H
NAME : WRDIVL / WRDIVH / WRDIVB
CONTENTS : DIVISOR & DIVIDEND BY DIVIDE

D7	D6	D5	D4	D3	D2	D1	D0	
MULTIPLIER-C (LOW)								4204H
C7	C6	C5	C4	C3	C2	C1	C0	
MULTIPLICAND-C (HIGH)								4205H
C15	C14	C13	C12	C11	C10	C9	C8	
DIVISOR-B								4206H
B7	B6	B5	B4	B3	B2	B1	B0	

- This is a register, which can set a Dividend (C) and a Divisor (B) for Absolute Divide of "C (16-BIT) ÷ B (8-BIT) = A (16-BIT)"
- The divisor (A) can be read by registers <4214H><4215H>. And the remainder can also be read by registers <4216H><4217H>.
- Set in the order of (C) and (B). The operation will start as soon as (B) has been set, and it will be completed right after 16-machine cycle period.
- Once the data of the A-REGISTER is set, it will not be destoroyed until new data is set.

ADDRESS : 4207H / 4208H
NAME : HTIMEL / HTIMEH
CONTENTS : H-COUNT TIMER SETTINGS

D7	D6	D5	D4	D3	D2	D1	D0	
H COUNT TIMER								4207H
H7	H6	H5	H4	H3	H2	H1	H0	
							H MSB H8	4208H

- This is a register. which can set the H-COUNT TIMER value.
- The setting value should be from 0 through 339. which is counted from the far left on the screen.
- When the coordinate counter becomes the count value set. the IRQ will be applied.
  And at the same time. "1" will be written to "timer IRQ" of register <4211H>. READ RESET>
  Enable/Disable of the interrupt will be determined by setting register <4200H>.

※ This countinuous counter is reset every scanning line. therefore once the count value is set. it is possible to apply the IRQ every time the scanning line comes to the same horizontal position on the screen.

ADDRESS : 4209H /420AH
NAME : VTIMEL / VTIMEH
CONTENTS : V-COUNT TIMER SETTINGS

D7	D6	D5	D4	D3	D2	D1	D0	
V-COUNT TIMER								4209H
V7	V6	V5	V4	V3	V2	V1	V0	
							V MSB V8	420AH

- This is a register. which can set the V-COUNT TIMER value.

  The setting value should be from 0 through 261(262). which is counted from the far top on the screen. (This line number described is different from the actual line number on the screen.)

- When the coordinate counter becomes the count value set. the IRQ will be applied.
  And at the same time. "1" will be written to "timer IRQ" of register <4211H>. READ RESET>
  Enable/Disable of the interrupt will be determined by setting register <4200H>.

※ This is a countinuous counter same as H-counter. and it will be reset every time 262(263) lines are scanned. Once the count value is set. it is possible to apply the IRQ every time the scanning line comes to the same vertical line on the screen.

ADDRESS : 420BH
NAME : MDMAEN
CONTENTS : CHANNEL DESIGNATION FOR GENERAL PURPOSE DMA & TRIGGER (START)

D7	D6	D5	D4	D3	D2	D1	D0
GENERAL PURPOSE DMA ENABLE FLAG							
CH7 EN	CH6 EN	CH5 EN	CH4 EN	CH3 EN	CH2 EN	CH1 EN	CH0 EN

420BH

- The General purpose DMA consists of 8-channels in total (CH0~ CH7).
- This register is used to designate the channel out of 8-channels (8-channels maximum).
- The channel which should be used can be designated by writting "1" to the bit of this channel. As soon as "1" is written to the bit (after a few cycles passed), the general purpose DMA transfer will be started.
- When the general purpose DMA of the designated channel is completed, the flag will be cleared.

NOTE : Because the data area (register <4300H> ~) of each channel is held in common with the data of each H-DMA channel, the channel designated by the H-DMA channel designation register <420CH> can not be used.
(It is prohibited to write "1" to the bit of the channel)
Therefore, 8-channels (CH0~CH7) should be assigned by the H-DMA and the general purpose DMA.

NOTE : If the H-Blank comes during the operation of the general purpose DMA and the H-DMA is started, the general purpose DMA will be discontinued in the middle, and re-started right after the H-DMA is complete.

NOTE : If 2 or more channels are designated, the DMA transfer will be performed continuously according to the priority order described by Appendix-1.
And also, the CPU stops operation until all the general purpose DMA are completed.

ADDRESS : 420CH
NAME : HDMAEN
CONTENTS : CHANNEL DESIGNATION FOR H-DMA

D7	D6	D5	D4	D3	D2	D1	D0
H-DMA ENABLE FLAG							
CH7 EN	CH6 EN	CH5 EN	CH4 EN	CH3 EN	CH2 EN	CH1 EN	CH0 EN

420CH

- The H-DMA consists of 8-channels in total (CH0~ CH7).
- This register is used to designate the channel out of 8-channels (8-channels maximum).
- The channel which should be used can be designated by writting "1" to the bit of this channel. As soon as H-Blank begins (after a few cycles passed), the H-DMA transfer will be started.

NOTE : Once this flag is set, it will not be destroyed (cleared) until new data is set.
Therefore, the initial settings are done automatically every field, and the same transfer pattern will be repeated.
And also, the flag is set out of V-BLANK period, the DMA transfer will be performed properly from next screen frame.

ADDRESS : 420DH
NAME : MEMSEL
CONTENTS : ACCESS CYCLE DESIGNATION IN MEMORY ② AREA

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
							2.68 3.58	420DH

ACCESS CYCLE DESIGNATION IN MEMORY② AREA

0 : 2.68MHz access cycle

1 : 3.58MHz access cycle (Only when the high speed memory is used)

- MEMORY ② shows the address (8000H ~ FFFFH) of the bank (80H~ BFH) and all the address of the bank (C0H ~ FFH).

- When power is turnes on or the reset signal is applied. it becomes "0".

ADDRESS : 4210H
NAME : #RDNMI
CONTENTS : NMI FLAG BY V-BLANK & VERSION NUMBER

D7	D6	D5	D4	D3	D2	D1	D0
BLANK NMI				5A22 VERSION NUMBER			

4210H

└ NMI FLAG BY V-BLANK : When "1" is written to "NMI ENABLE" of register <4200H>, this flag will show NMI status.
  ┌ 0 : NMI status is "Disable"
  └ 1 : NMI status is "Enable"

※※ "1" is set to this flag at beginning of V-Blank, and "0" is set at end of V-Blank.
Also, it can be set by reading this register.

NOTE : It is necessary to reset by reading this flag during NMI processing. (See Appendix-3)

ADDRESS : 4211H
NAME : #TIMEUP
CONTENTS : IRQ FLAG BY H/V COUNT TIMER

D7	D6	D5	D4	D3	D2	D1	D0
TIMER IRQ							

4211H

└ IRQ FLAG BY H/V COUNT TIMER
: (In case the Timer Enable is set by "Timer Enable" of register <4200H>:)
as soon as H/V counte timer becomes the count value set, IRQ will be applied and "1" will be set to this flag.
This flag is "READ-RESET".

※※ Even if V-EN="0" and H-EN="0" are set by "Timer Enable" of register <4200H>, this flag will be reset.
  ┌ 0 : Either H/V count Timer is in active or disable
  └ 1 : H/V Count Timer is Time-Up

ADDRESS : 4212H
NAME : #HVBJOY
CONTENTS : H/V BLANK FLAG & JOY CONTROLLER ENABLE FLAG

D7	D6	D5	D4	D3	D2	D1	D0
V BLANK	H BLANK						JOY-C ENABLE

4212H

JOY CONTROLLER ENABLE FLAG
: This flag shows the timing to read the data of the Joy Controller. (However, it is limited to the case which the "JOY-C ENABLE" of register <4200H> is set to "1".)

- 0 : This is a period that the Joy Controller is not reading the data or the Joy Controller is disabled. (In case "0" is set to "JOY-C ENABLE" of register <4200H>)
- 1 : This is a period that the Joy Controller is reading the data.

H-BLANK PERIOD FLAG : It shows whether the scanning is in the H-Blank period or not.

- 0 : Out of H-BLANK period
- 1 : In H-BLANK period

V-BLANK PERIOD FLAG : It shows whether the scanning is in the period of V-Blank or not.

- 0 : Out of V-BLANK period
- 1 : In V-BLANK period

ADDRESS : 4213H
NAME : #RDIO
CONTENTS : PROGRAMABLE I/O PORT (IN-PORT)

D7	D6	D5	D4	D3	D2	D1	D0
I/O PORT							
D7	D6	D5	D4	D3	D2	D1	D0

4213H

- This is a Programable I/O port (IN-PORT). The data which is set to the IN-PORT should be read directly.
- The bit which "1" is written by register <4201H> is used as the IN-PORT.

ADDRESS : 4214H / 4215H
NAME : *RDDIVL / *RDDIVH
CONTENTS : QUOTIENT OF DIVIDE RESULT

D7	D6	D5	D4	D3	D2	D1	D0	
QUOTIENT-A (LOW)								4214H
A7	A6	A5	A4	A3	A2	A1	A0	
QUOTIENT-A (HIGH)								4215H
A15	A14	A13	A12	A11	A10	A9	A8	

- This is a Quotient (A), which is a result for Absolute Divide of
  " C (16-BIT) ÷ B (8-BIT) = A (16-BIT)"
- Dividend (C) and Divisor (B) are set by registers <4204H> <4205H> <4206H>.

ADDRESS : 4216H / 4217H
NAME : *RDMPYL / *RDMPYH
CONTENTS : PRODUCT OF MULTIPLICATION RESULT OR REMAINDER OF DIVIDE RESULT

D7	D6	D5	D4	D3	D2	D1	D0	
PRODUCT-C (MULTIPLICATION) / REMAINDER (DIVIDE) (LOW)								4216H
C7	C6	C5	C4	C3	C2	C1	C0	
PRODUCT-C (MULTIPLICATION) / REMAINDER (DIVIDE) (HIGH)								4217H
C15	C14	C13	C12	C11	C10	C9	C8	

① IN CASE OF MULTIPLICATION
- This is a Product (C) which is a result for Absolute Multiplication of
  " A (8-BIT) × B (8-BIT) = C (16-BIT)"
- A Multiplicand (A) and a Multiplier (B) are set by registers <4202H> <4203H>.

② IN CASE OF DIVIDE
- This is a Remainder which is a result for the Absolute Divide of
  " C (16-BIT) ÷ B (8-BIT) = A (16-BIT) · · · REMAINDER (8 or 16-Bit)"
- A Dividend (C) and a Divisor (B) are set by the registers <4204H> <4205H> <4206H>.

ADDRESS : 4218H / 4219H / 421AH / 421BH / 421CH / 421DH / 421EH / 421FH
NAME : JOY1L / JOY1H / JOY2L / JOY2H / JOY3L / JOY3H / JOY4L / JOY4H
CONTENTS : DATA FOR JOY CONTROLLER I. II. III. & IV

	D7	D6	D5	D4	D3	D2	D1	D0
4218H	JOY CONTROLLER-I (LOW)							
	A BUTTON	X BUTTON	TL BUTTON	TR BUTTON				
4219H	JOY CONTROLLER-I (HIGH)							
	B BUTTON	Y BUTTON	SELECT BUTTON	START BUTTON	JOY PAD UP	JOY PAD DOWN	JOY PAD LEFT	JOY PAD RIGHT
421AH	JOY CONTROLLER-II (LOW)							
	X BUTTON	Y BUTTON	TL BUTTON	TR BUTTON				
421BH	JOY CONTROLLER-II (HIGH)							
	A BUTTON	B BUTTON	SELECT BUTTON	START BUTTON	JOY PAD UP	JOY PAD DOWN	JOY PAD LEFT	JOY PAD RIGHT
421CH	JOY CONTROLLER-III (LOW)							
421DH	JOY CONTROLLER-III (HIGH)							
	A BUTTON	B BUTTON	SELECT BUTTON	START BUTTON	JOY PAD UP	JOY PAD DOWN	JOY PAD LEFT	JOY PAD RIGHT
421EH	JOY CONTROLLER-IV (LOW)							
421FH	JOY CONTROLLER-IV (HIGH)							
	A BUTTON	B BUTTON	SELECT BUTTON	START BUTTON	JOY PAD UP	JOY PAD DOWN	JOY PAD LEFT	JOY PAD RIGHT

EXPANDED CONNECTOR

$09 up or Right
$04 up or Left

- Registers <4016H> <4017H> can be used the same as the Family Computer.

PORT	D7	D6	D5	D4	D3	D2	D1	D0
4016H RD								
4016H WR								
4017H RD								

4016H D0 : Data for Controller I
4016H D1 : Data for Controller III
OUT0. OUT1. OUT2
4017H D0 : Data for Controller II
4017H D1 : Data for ControllerIV

NOTE : Whether the standard joy controllers are connected to the SFX unit or not can be reffered by reading 17th bit of 4016H 4017H
- 0 : connected
- 1 : not connected

ADDRESS : 43XOH (X : CHANNEL NUMBER <0 ~7>)
NAME :
CONTENTS : PARAMETER FOR DMA TRANSFER

D7	D6	D5	D4	D3	D2	D1	D0	
CH	CH		A BUS ADDRESS		CH TRANSFER WORD SELECT			43×0H
*	TYPE		INC/DEC	FIXED	D2	D1	D0	

DMA TRANSFER WORD SELECT

*: Transfer Origination

GENERAL PURPOSE DMA : B-ADDRESS CHANGE METHOD DESIGNATION PER CHANNEL

D2	D1	D0	ADRESS TO BE WRITTEN
0	0	0	1-ADDRESS
0	0	1	2-ADDRESS (VRAM etc.) L.H
0	1	0	1-ADDRESS
0	1	1	2-ADDRESS (WRITE TWICE) L.L.H.H
1	0	0	4-ADDRESS L.H.L.H

H-DMA : The number of byte to be transfered per line and write method designation

D2	D1	D0	# OF BYTE TO BE TRANSFERED	ADRESS TO BE WRITTEN		
0	0	0	1 - BYTE	1-ADDRESS		(1)
0	0	1	2 - BYTE	2-ADDRESS (VRAM etc.)	L. H	(2)
0	1	0	3 - BYTE	WITE TWICE	L. L	(1)
0	1	1	4 - BYTE	2-ADDRESS WRITE TWICE	L.L.H.H	(2)
1	0	0	4 - BYTE	4-ADDRESS	L.H.L.H	(4)

FIXED ADDRESS FOR A-BUS & AUTOMATIC INCREMENT/DECREMENT SELECT (IN CASE OF GENERAL PURPOSE DMA)

D3
- 0 : AUTOMATIC ADDRESS INCREMENT/DECREMENT
- 1 : FIXED ADDRESS <To be used when clearing VRAM etc.>

D4 (In case "0" is written to D3)
- 0 : AUTOMATIC INCREMENT
- 1 : AUTOMATIC DECREMENT

TYPE DESIGNATION (H-DMA ONLY) : Addressing mode designation when accessing the data <See Appendix-2>
- 0 : ABSOLUTE ADDRESSING
- 1 : INDIRECT ADDRESSING

TRANSFER ORIGINATION DESIGNATION : Transfer Direction A Bus—B Bus, B Bus—A Bus Designation <See Appendix-1>
- 0 : A-BUS — B-BUS (CPU MEMORY — PPU)
- 1 : B-BUS —A-BUS (PPU — CPU MEMORY)

※ For example, in case the DMA transfer is performed from CPU memory to PPU, "0" should be written.

A; 0 -> 4300

4 -> 4301 -> (2104)
0 -> 4302
0C -> 4303 } Adress
7E -> 4304

0080 -> 4305 # of bytes
0000 -> 2101 adress in OAM to copy to
01 -> 420B start dma

ADDRESS : 43X1H (X : CHANNEL NUMBER <0 ~7>)
NAME :
CONTENTS : B-BUS ADDRESS FOR DMA

D7	D6	D5	D4	D3	D2	D1	D0	
B-ADDRESS								43×1H
BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0	

- This is a register, which can set the address of B-bus.
- Whether this is the address of the "Transfer Desitination" or the address of the "Transfer Origination" can be determined by D7 (Transfer Origination) of register <4300H>.

A-BUS ——— Direction can be designated by "Transfer Origination" ——— B-BUS
Actual address is 0021XXH.
(XX : value by this register)

※ When the H-DMA is performed, it will be the address of the "Transfer Desitination".

ADDRESS : 43X2H / 43X3H / 43X4H (X : CHANNEL NUMBER <0 ~7>)
NAME :
CONTENTS : TABLE ADDRESS OF A-BUS FOR DMA <A1 TABLE ADDRESS>

D7	D6	D5	D4	D3	D2	D1	D0	
A1 TABLE ADDRESS (LOW)								43×2H
A7	A6	A5	A4	A3	A2	A1	A0	
A1 TABLE ADDRESS (HIGH)								43×3H
A15	A14	A13	A12	A11	A10	A9	A8	
A-TABLE BANK								43×4H
A23	A22	A21	A20	A19	A18	A17	A16	

- This is a register, which can set the address of A-bus.
- Whether this is the address of the "Transfer Desitination" or the address of the "Transfer Origination" can be determined by D7 (Transfer Origination) of register <4300H>.
  "0" should be written to D7 except a special case.
- In the H-DMA mode, the address of the transfer origination is designated except a special case. Therefore, for the CPU area designated by this address, the data (Appendix-2) must be set by the absolute addressing mode or the indirect addressing mode.
- This address becomes the basic address on the A-Bus during DMA transfer period, and the address will be increased or decreased based on this address.
  (When the general purpose DMA is performed, it will be decreased.)

ADDRESS : 43X5H / 43X6H / 43X7H (X : CHANNEL NUMBER <0 ~7>)
NAME :
CONTENTS : DATA ADDRESS STORE BY H-DMA
& NUMBER OF BYTE TO BE TRANSFERED SETTINGS BY GENERAL PURPOSE DMA

D7	D6	D5	D4	D3	D2	D1	D0	
DATA ADDRESS (LOW)								(In case of H-DMA) 43×5H
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	
NUMBER OF BYTE TO BE TRANSFERED (LOW)								(In case of General Purpose DMA)
B7	B6	B5	B4	B3	B2	B1	B0	

DATA ADDRESS (HIGH)								(In case of H-DMA) 43×6H
DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8	
NUMBER OF BYTE TO BE TRANSFERED (HIGH)								(In case of General Purpose DMA)
B15	B14	B13	B12	B11	B10	B9	B8	

DATA BANK								(In case of H-DMA) 43×7H
DA23	DA22	DA21	DA20	DA19	DA18	DA17	DA16	

- IN CASE OF H-DMA
  This is a register which the indirect address will be stored automatically in the Indirect addressing mode.
  The indirect address means the Data Address described on Appendix-2.
  It is not necessary to read or write directly by the CPU except in special cases.

- IN CASE OF GENERAL PURPOSE DMA
  This is the register, which can set the number of byte to transfer or to be transfered.
  However, the number of Byte (0000H) means 10000H.

ADDRESS : 43X8H / 43X9H (X : CHANNEL NUMBER <0 ~7>)
NAME :
CONTENTS : TABLE ADDRESS OF A-BUS BY DMA <A2 Table Address>

D7	D6	D5	D4	D3	D2	D1	D0	
A2 TABLE ADDRESS (LOW)								43×8H
A7	A6	A5	A4	A3	A2	A1	A0	
A2 TABLE ADDRESS (HIGH)								43×9H
A15	A14	A13	A12	A11	A10	A9	A8	

- This is the address, which is used to access the CPU and RAM, and it will be increased automatically. (See Appendix-2)
- The data of this register is used as the basic address which is the address set by the "A2 Table Address". Afterwards, because it will be increased (or decreased) automatically, it is necessary to set the address into this register by the CPU directly.

  However, if the data which is transfered needs to be changed by force, it can be done by setting the CPU memory address to this register. And also, the address of the CPU which is accessed currently will be changed by reading this register. — H-DMA ONLY

ADDRESS : 43XAH (X : CHANNEL NUMBER <0 ~7>)
NAME :
CONTENTS : THE NUMBER OF LINE TO BE TRANSFERED BY H-DMA

D7	D6	D5	D4	D3	D2	D1	D0	
CON-TINUE	NUMBER OF LINE							43×AH
	L6	L5	L4	L3	L2	L1	L0	

- This is a register which shows number of line for H-DMA transfer. See Appendix-2)
- The number of line written to the CPU memory will be the basic number of line. it is not necessary to set the address into this register by the CPU directly.

SUPER FAMICOM

REGISTER (CPU)

* * * * APPENDIX * * * *

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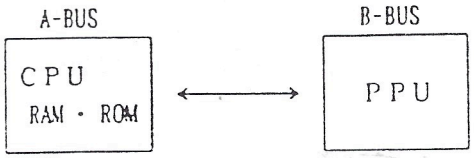
GENERAL PURPOSE DMA

(i) TRANSFER METHOD



(ii) DATA FORMAT

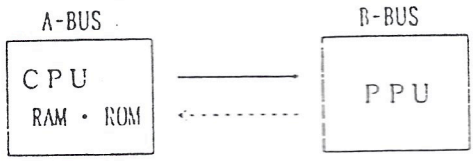
TYPICAL DATA BANK

(iii) TRIGGER (START)

GENERAL PURPOSE DMA ENABLE FLAG

H-DMA

(i) TRANSFER METHOD



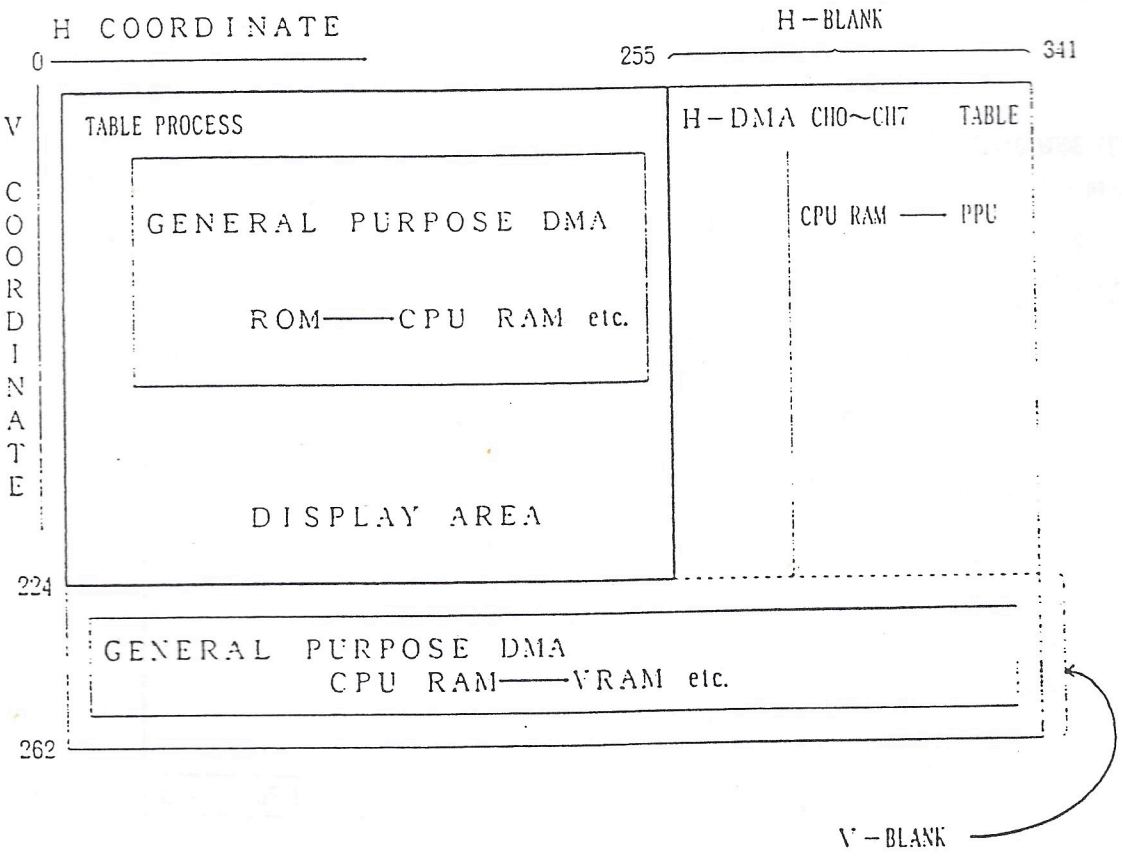
(ii) DATA FORMAT (See Appendix-3 & 4)

- TYPE 0 : Absolute addressing
- TYPE 1 : Indirect Addressing
  - C "0" : If the data is same as the data of previous line, the data will not be transfered. (Data Compression)
  - C "1" : A pair of data per horizontal line

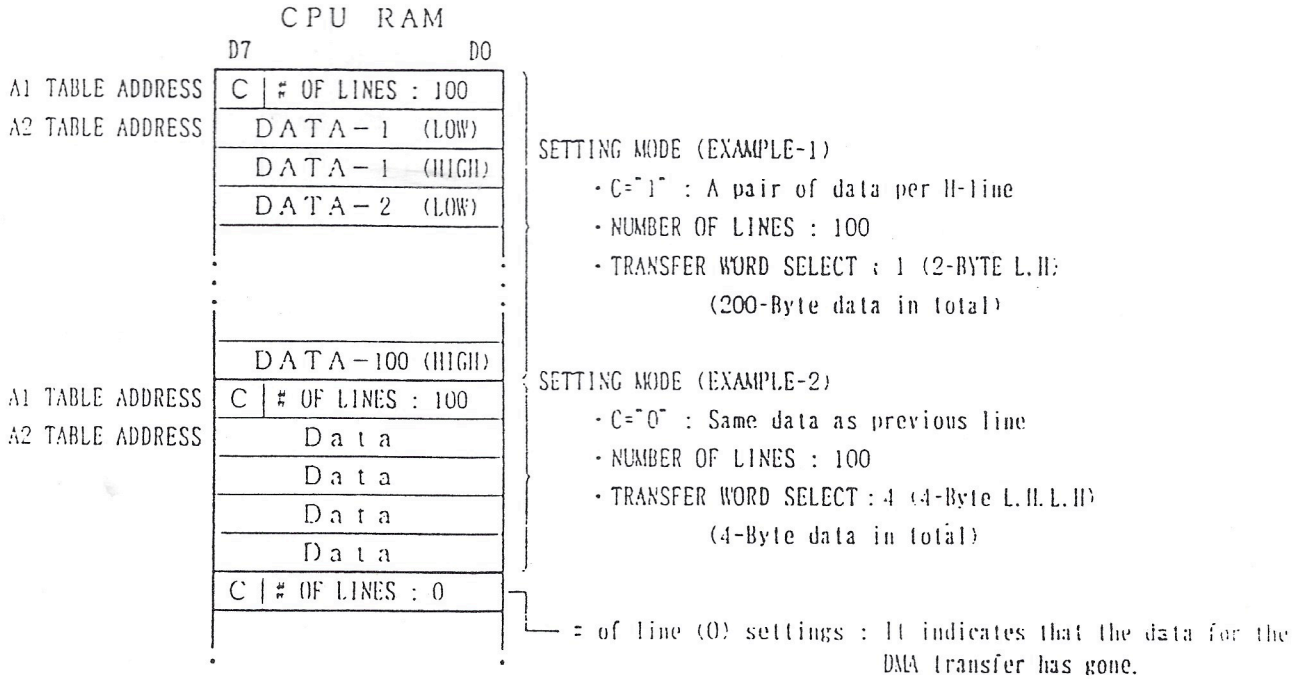
(iii) TRIGGER (START)

H-BLANK

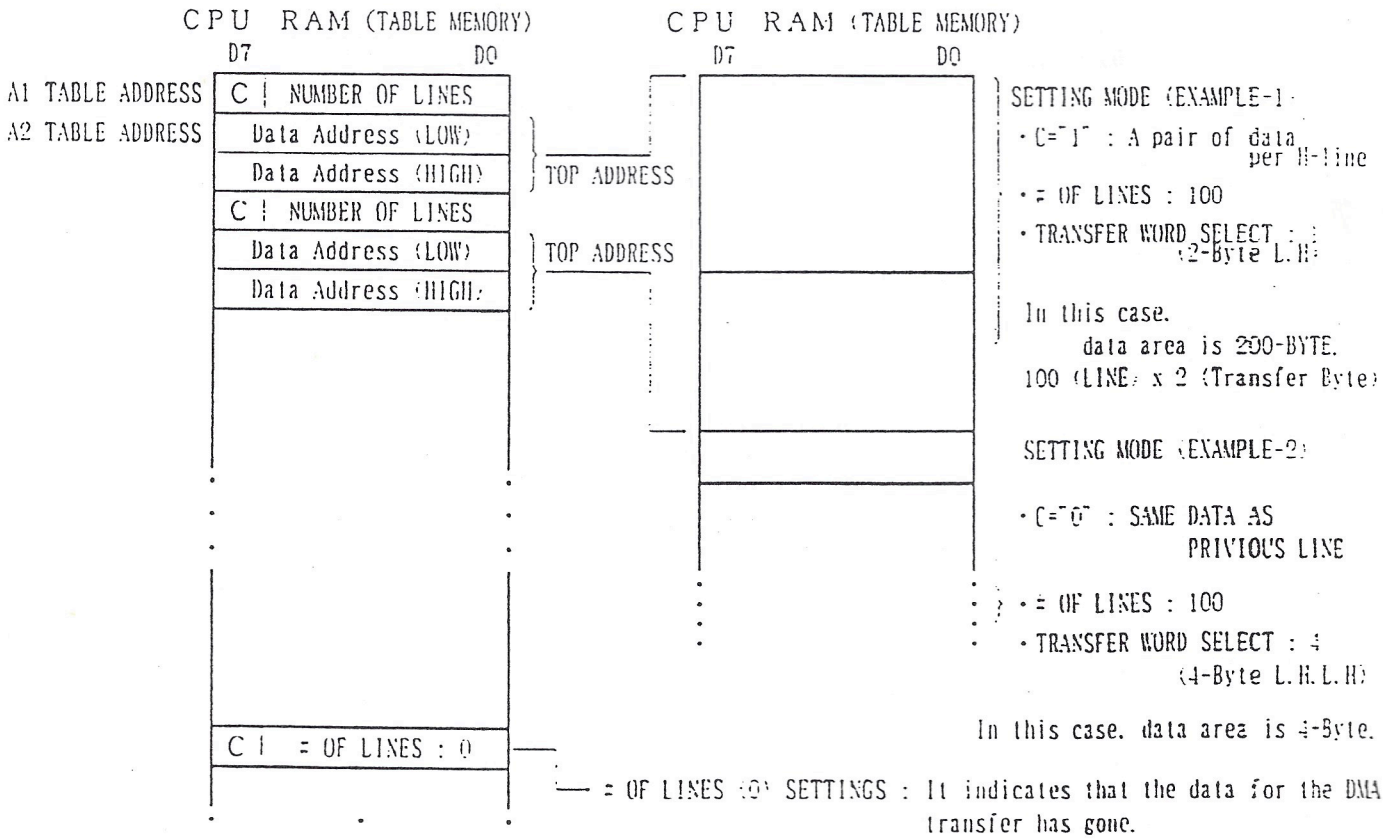
PRIORITY
- H-DMA > GENERAL PURPOSE DMA
- ch 0 > ch 1 > · · · > ch 7
  in the same DMA (General purpose DMA or H-DMA)



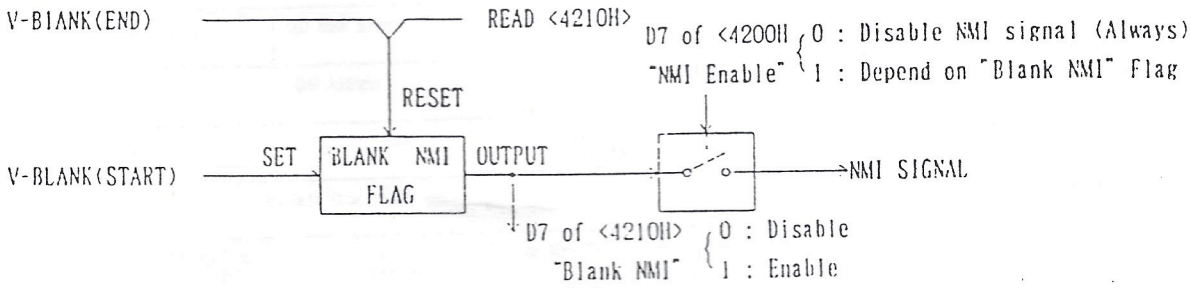
ABSOLUTE ADDRESSING (TYPE-0) ····· This is a mode to transfer the data of the address designated by the TABLE ADDRESS.


CPU RAM
D7
D0
A1 TABLE ADDRESS
A2 TABLE ADDRESS
C | # OF LINES : 100
DATA-1 (LOW)
DATA-1 (HIGH)
DATA-2 (LOW)
DATA-100 (HIGH)
A1 TABLE ADDRESS
A2 TABLE ADDRESS
C | # OF LINES : 100
Data
Data
Data
Data
C | # OF LINES : 0
SETTING MODE (EXAMPLE-1)
・C="1" : A pair of data per H-line
・NUMBER OF LINES : 100
・TRANSFER WORD SELECT : 1 (2-BYTE L.H)
(200-Byte data in total)
SETTING MODE (EXAMPLE-2)
・C="0" : Same data as previous line
・NUMBER OF LINES : 100
・TRANSFER WORD SELECT : 4 (4-Byte L.H.L.H)
(4-Byte data in total)
= of line (0) settings : It indicates that the data for the DMA transfer has gone.

INDIRECT ADDRESSING (TYPE-1) ····· This is a mode to transfer the data of the address designated by the Data Address. which is stored to the address designated by the Table Address.


CPU RAM (TABLE MEMORY)
D7
D0
A1 TABLE ADDRESS
A2 TABLE ADDRESS
C | NUMBER OF LINES
Data Address (LOW)
Data Address (HIGH)
TOP ADDRESS
C | NUMBER OF LINES
Data Address (LOW)
Data Address (HIGH)
TOP ADDRESS
C | = OF LINES : 0
CPU RAM (TABLE MEMORY)
D7
D0
SETTING MODE (EXAMPLE-1)
・C="1" : A pair of data per H-line
・= OF LINES : 100
・TRANSFER WORD SELECT : 1 (2-Byte L.H)
In this case.
data area is 200-BYTE.
100 (LINE) x 2 (Transfer Byte)
SETTING MODE (EXAMPLE-2)
・C="0" : SAME DATA AS PRIVIOUS LINE
・= OF LINES : 100
・TRANSFER WORD SELECT : 4 (4-Byte L.H.L.H)
In this case. data area is 4-Byte.
= OF LINES (0) SETTINGS : It indicates that the data for the DMA transfer has gone.

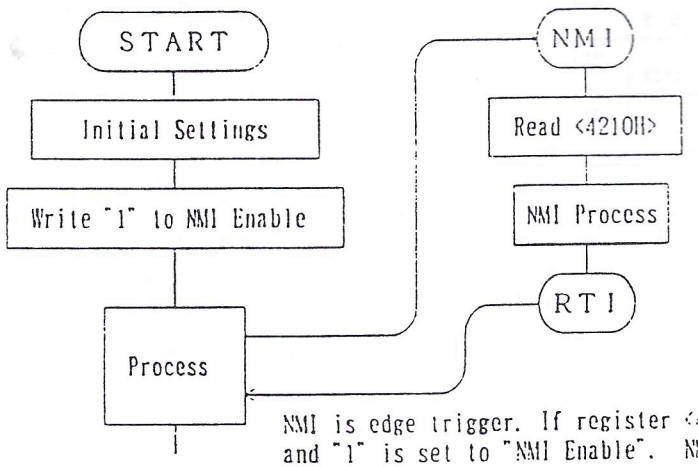
DETECT BEGINNING OF V-BLANK



The "Blank NMI" flag of register <4210H> will be set at beginning of V-Blank and will be reset at end of V-Blank. Also, it can be reset by reading register <4210H>.

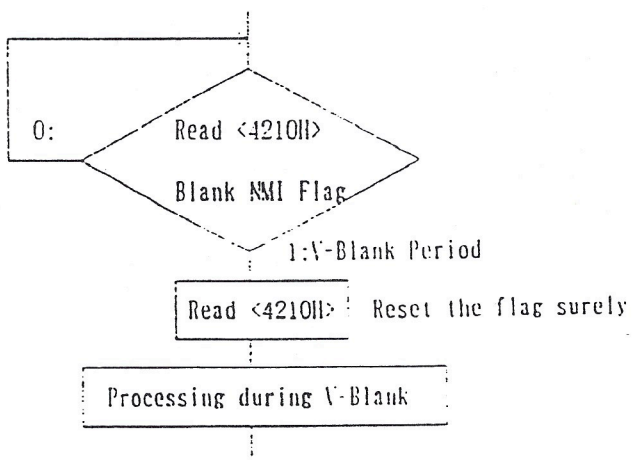
<EXAMPLE>

1. In case of detecting the beeginning of V-Blank by NMI:



NMI is edge trigger. If register <4210H> is not read during and "1" is set to "NMI Enable", NMI will be duplicated.

2. In case of detecting the beginning of V-Blank by the flag



SUMMARY OF REGISTERS

REGISTERS (WRITE) S-PPU

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
2100H	Blanking				Fade IN/OUT (0 ~15)			
2101H	OBJ Size Select			OBJ Name Select		OBJ Name Base Address		
2102H	OAM Address							
2103H	OAM Priority Rotation							OAM Address MSB
2104H	OAM Data (Low, High)							
2105H	BG4	BG 16 x 16 Size BG3	BG2	BG1	BG3 Priority	BG Mode (0~ 7)		
2106H	Mosaic Size				Mosaic Enable BG4	BG3	BG2	BG1
2107H	BG1 SC Base Address							BG1 SC Size
2108H	BG2 SC Base Address							BG2 SC Size
2109H	BG3 SC Base Address							BG3 SC Size
210AH	BG4 SC Base Address							BG4 SC Size
210BH	BG2 Name Base Address				BG1 Name Base Address			
210CH	BG4 Name Base Address				BG3 Name Base Address			
210DH	BG1 H-Offset (Low, High)							
210EH	BG1 V-Offset (Low, High)							
210FH	BG2 H-Offset (Low, High)							
2110H	BG2 V-Offset (Low, High)							
2111H	BG3 H-Offset (Low, High)							
2112H	BG3 V-Offset (Low, High)							
2113H	BG4 H-Offset (Low, High)							
2114H	BG4 V-Offset (Low, High)							
2115H	H-L Inc.				V-RAM Address Sequence Mode Full Graphic		SC Increment	
2116H	V-RAM Address (Low)							
2117H	V-RAM Address (High)							
2118H	V-RAM Data (Low)							
2119H	V-RAM Data (High)							
211AH	Screen Over							Screen Flip V H

REGISTERS (WRITE) S-PPU

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
211BH	Matrix Parameter A (Low, High)							
211CH	Matrix Parameter B (Low, High)							
211DH	Matrix Parameter C (Low, High)							
211EH	Matrix Parameter D (Low, High)							
211FH	Center Position X (Low, High)							
2120H	Center Position Y (Low, High)							
2121H	CG-RAM Address							
2122H	CG-RAM Data (Low, High)							
2123H	W2 EN	BG2 Window IN/OUT	W1 EN	IN/OUT	W2 EN	BG2 Window IN/OUT	W1 EN	IN/OUT
2124H	W2 EN	BG2 Window IN/OUT	W1 EN	IN/OUT	W2 EN	BG2 Window IN/OUT	W1 EN	IN/OUT
2125H	W2 EN	Color Window IN/OUT	W1 EN	IN/OUT	W2 EN	Color Window IN/OUT	W1 EN	IN/OUT
2126H	Window W0 Position (0 ~ 255)							
2127H	Window W1 Position (0 ~ 255)							
2128H	Window W2 Position (0 ~ 255)							
2129H	Window W3 Position (0 ~ 255)							
212AH	BG4	BG3	window Logic BG2	BG1				
212BH					Window Logic Color	OBJ		
212CH				OBJ	Through Main BG4	BG3	BG2	BG1
212DH				OBJ	Through Sub BG4	BG3	BG2	BG1
212EH				OBJ	Through Main (Window) BG4	BG3	BG2	BG1
212FH				OBJ	Through Sub (Window) BG4	BG3	BG2	BG1
2130H	Window ON/OFF Main SF (A)		Sub SF (B)				CG ADD Enable	Direc Selec
2131H	ADD/SUB	Half	ADD or SUB Enable OBJ	BG4	BG3	BG2	BG1	
2132H	Blue	Green	Red	Color Constant Data	Color Brilliance Data			
2133H	EXT. Sync	EXT. Input		Pseudo 512	224/239	OBJ-V Select	Inter	
2134H	MPY (Low)							
2135H	MPY (Mid)							
2136H	MPY (High)							

REGISTER (READ) S-PPU

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
2137H	Soft Latch for H/V Counter							
2138H	OAM Data (Low, High)							
2139H	V-RAM Data (Low)							
213AH	V-RAM Data (High)							
213BH	CG Data (Low, High)							
213CH	Output Data of H-Counter (Low, High)							
213DH	Output Data of V-Counter (Low, High)							
213EH	Time Over	Range Over	Master /Slave		5C77 Version Number			
213FH	Field	EXT Latch		NTSC/PAL	5C78 Version Number			
2140H	APU I/O Port							
2141H	APU I/O Port							
2142H	APU I/O Port							
2143H	APU I/O Port							

REGISTERS (WRITE) S-CPU

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
4200H	NMI Enable		Timer Enable V-EN	H-EN				Joy-C Enable
4201H	I/O Port							
4202H	Multiplicand-A							
4203H	Multiplier-B							
4204H	Dividend-C (Low)							
4205H	Dividend-C (High)							
4206H	Divisor-B							
4207H	V-Counter Timer							
4208H								H-MSB
4209H	V-Counter Timer							
420AH								V-MSB
420BH	General Purpose DMA Enable Flag: DM EN, D6 EN, D5 EN, D4 EN, D3 EN, D2 EN, D1 EN, D0 EN							
420CH	H-DMA Enable Flag: DM EN, D6 EN, D5 EN, D4 EN, D3 EN, D2 EN, D1 EN, D0 EN							
420DH								2.68 / 3.58

REGISTERS (READ) S-CPU

ADDRESS	D7	D6	D5	D4	D3	D2	D1	
4210H	Blank /NMI					5A22 Version Number		
4211H	Timer IRQ							
4212H	V-Blank	H-Blank						Jo Er
4213H	I/O Port							
4214H	Quotient (Low)							
4215H	Quotient (High)							
4216H	Product-C / Remainder (Low)							
4217H	Product-C / Remainder (High)							
4218H	Joy Controller I (Low)							
4219H	Joy Controller I (High)							
421AH	Joy Controller II (Low)							
421BH	Joy Controller II (High)							
421CH	Joy Controller III (Low)							
421DH	Joy Controller III (High)							
421EH	Joy Controller IV (Low)							
421FH	Joy Controller IV (High)							

REGISTERS (WRITE) S-CPU

CX : Channel <0

ADDRESS	D7	D6	D5	D4	D3	D2	D1	
43X0H	CHX * T-Org	CHX Type		A-Bus Address INC/DEC	Fixed	CHX Transfer Word Sel		
43X1H	CHX B-Address							
43X2H	CHX A1 Table Address (Low)							
43X3H	CHX A1 Table Address (High)							
43X4H	CHX A-Table Bank							
43X5H	CHX Data Address (H-DMA) / Number of Byte to be transfered (General purpose DMA)							
43X6H	CHX Data Address (H-DMA) / Number of Byte to be transfered (General purpose DMA)							
43X7H	CHX Data Bank (H-DMA)							
43X8H	CHX A2 Table Address (Low)							
43X9H	CHX A2 Table Address (High)							
43XAH	Continue	Number of Line						

Note : T-Org means the "Transfer Origination".

SUPER FAMICOM SOUND

PROGRAMMING MANUAL

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1. SFX SOUND SOURCE OUTLINE

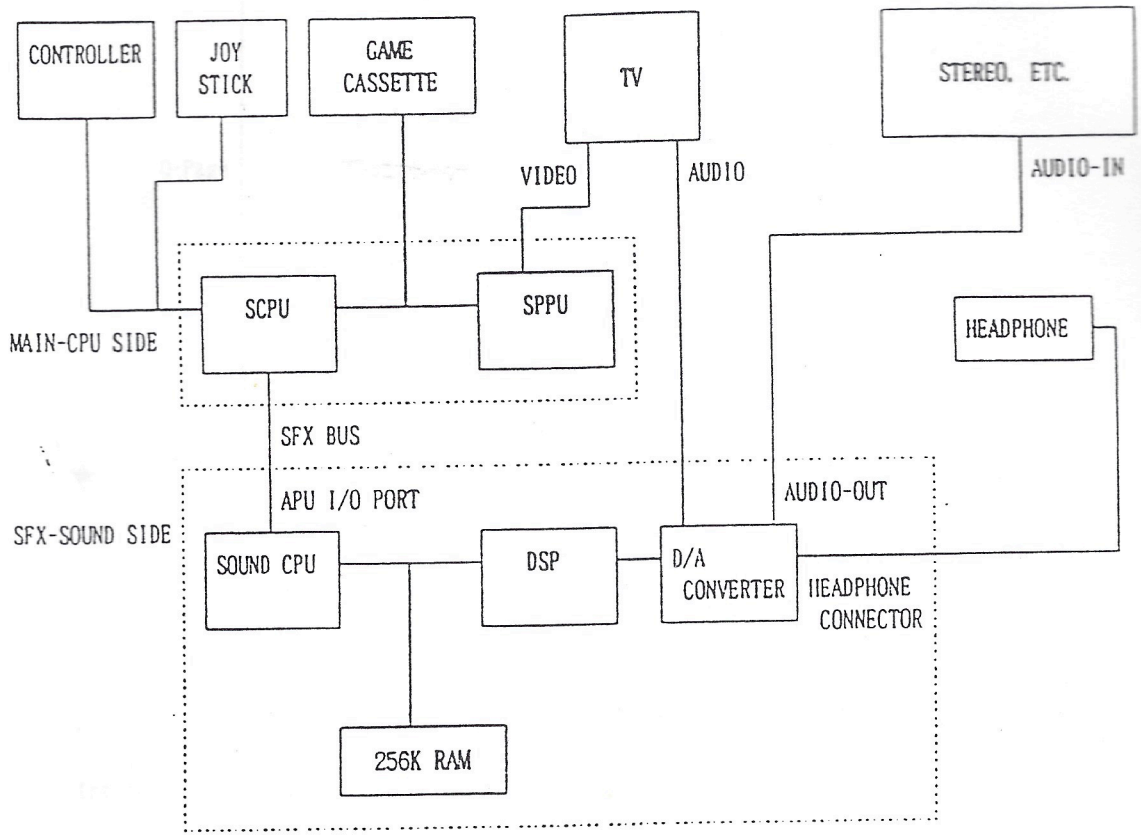
1.1 OUTLINE

The SFX sound source is composed of a Sound-CPU-IC. a single chip in which are integrated an 8-bit CPU. IPL ROM. I/O ports and timers. a DSP-IC and peripheral apparatus.

CHARACTERISTICS

・CPU	: Sony SPC700 series CMOS 8-bit CPU core
・Minimum Command Execution Time	: 1.953 μs/2.048MHz when active
・Internal ROM	: 64 byte (IPL ROM)
・Memory Space	: 64K byte
・Peripheral Functions	
・I/O Ports	: SCPU Interface I/O Ports 8 bit x 4 Universal I/O Ports 8 bit x 2
・Timers	: (8 bit timer + 4 bit counter) x 3 sets
・Output Sound Production	: 4-bit ADPCM sampling sound x 8 tones (simultaneous production)

1.2. SYSTEM OUTLINE



Designation & Role of Each Section:

Sound-CPU: SFX sound source CPU. Program and tone color data are read into RAM from the game cassette through the SCPU, consequently controlling the game music.
In addition, provided with an internal IPL-ROM which is activated upon rest, transmission of data through the SCPU, initial settings of the SFX sound source, etc., are carried out.

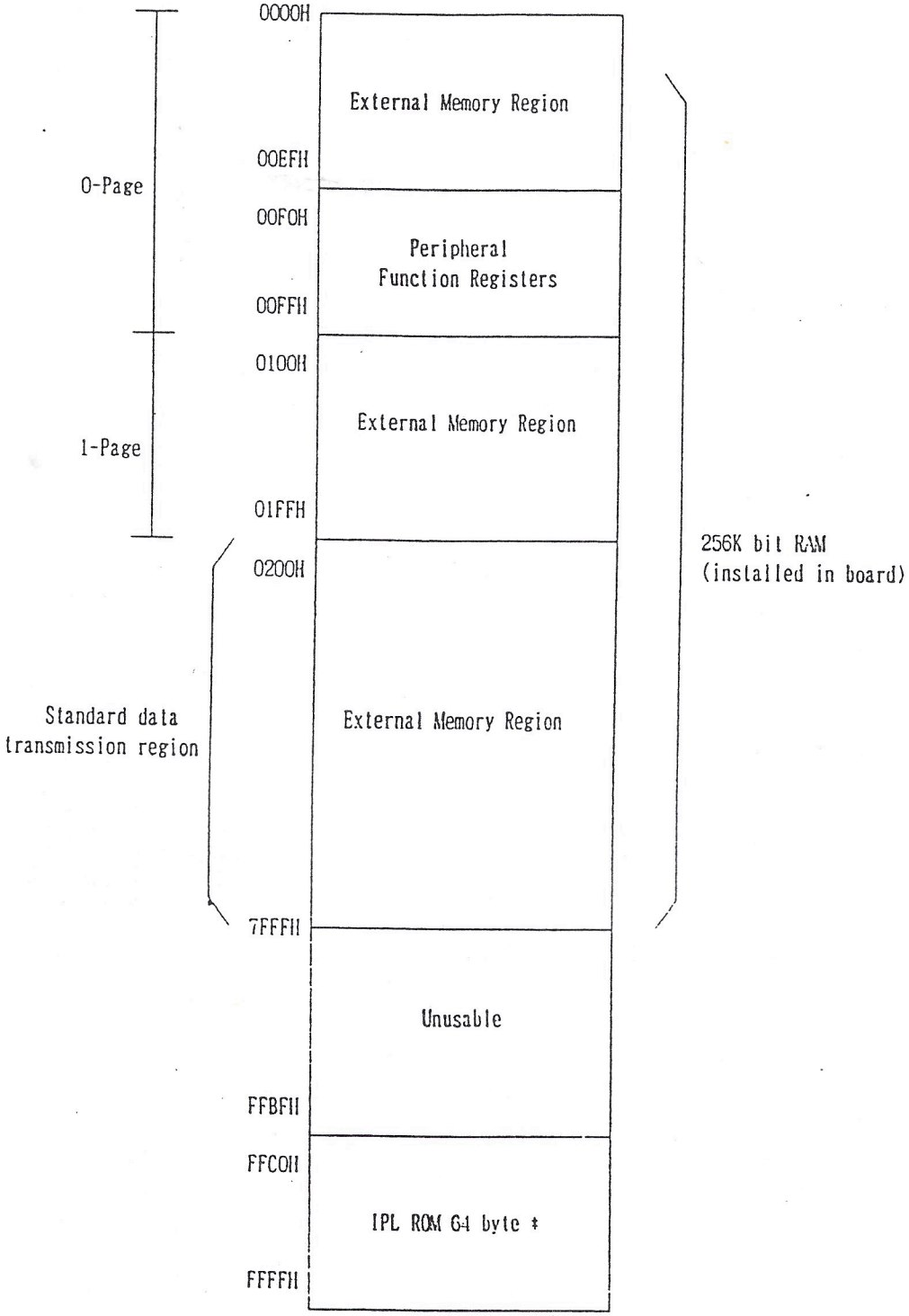
DSP: Digital signal processor. Reproduces tone quality data in RAM. Possesses various functions for the purpose of musical expression.

256K RAM : Shared on a time basis by the Sound-CPU and the DSP.

SPCU : CPU for SFX use. Carries out progression of the game in conformity with the game cassette program.

SPPU : PPU for SFX use. Creates imaging through CPU control.

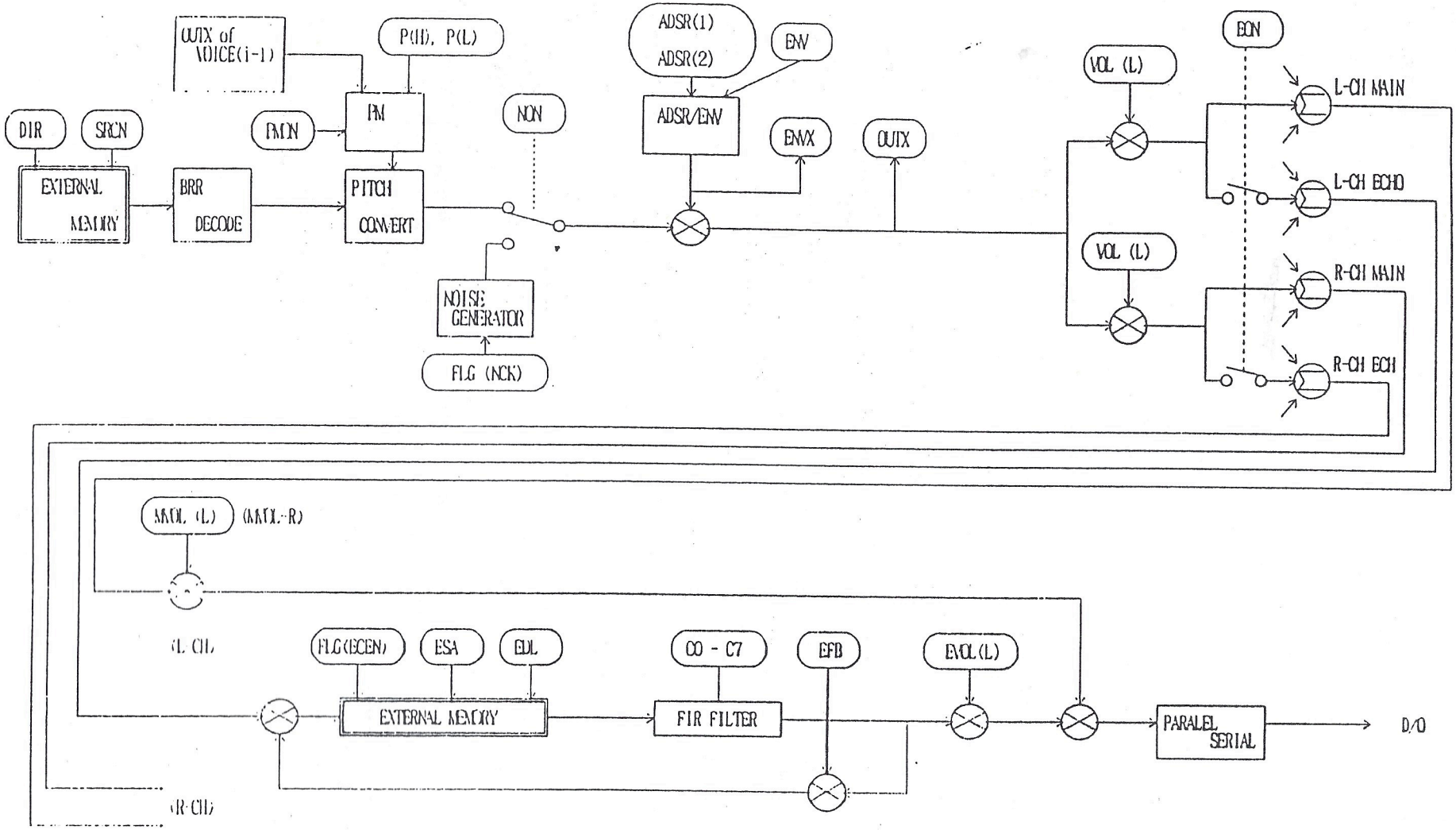
1.3. MEMORY MAPPING



* The initial hardware setting program is installed in the IPL ROM

1.4. SIGNAL FLOW

<NOA-SFX-01/15/00>



2. I/O PORTS

2.1. PERIPHERAL FUNCTIONS REGISTERS

Peripheral Function Registers

Address	Function Register	R/W	When Reset	Remarks
00F0H	(test)	---	------	Installed in sound-CPU
00F1H	Control	W	Control = "--00-000"	
00F2H	Register Add.	R/W	Indeterminate	Installed in DSP
00F3H	Register Data	R/W	Indeterminate	Installed in DSP
00F4H	Port-0	R/W	Port0r = "00" Port0w = "00"	Installed in sound-CPU
00F5H	Port-1	R/W	Port1r = "00" Port1w = "00"	Installed in sound-CPU
00F6H	Port-2	R/W	Port2r = "00" Port2w = "00"	Installed in sound-CPU
00F7H	Port-3	R/W	Port3r = "00" Port3w = "00"	Installed in sound-CPU
00F8H	-----	---	----------	----------
00F9H	-----	---	----------	----------
00FAH	Timer-0	W	Indeterminate	Installed in sound-CPU
00FBH	Timer-1	W	Indeterminate	Installed in sound-CPU
00FCH	Timer-2	W	Indeterminate	Installed in sound-CPU
00FDH	Counter-0	R	Indeterminate	Installed in sound-CPU
00FEH	Counter-1	R	Indeterminate	Installed in sound-CPU
00FFH	Counter-2	R	Indeterminate	Installed in sound-CPU

2.2. APU I/O PORTS

Ports 0-3 are ports which carry out data transmission to the SPCU through the SFX bus and are composed of four 8-bit inport registers and four 8-bit outport registers. Port nr registers can only write from the SPCU section and can only read from the Sound-CPU section. The opposite is true of the port nw registers. Since the composition of ech of these ports is identical, an explanation will be made using Port Or and Port Ow as examples.

1. Data is input into Port Or when the SCPU writes data into 2140H. Then, the contents of Ports Or are read when the Sound-CPU reads the data in 00F4H (this is also true of Ports 1r - 3r).
2. Data is written into Port Ow when the Sound-CPU writes data into the APU I/O port (00F4H). Then, the contents of Port Ow are read when the SCPU reads 2140H (this is also true of Ports 1w - 3w).
3. When reset is carried out, the contents of Port nr registers and Port nw registers become "00" (n=0-3).

Table 2.1.1. Port0 - Port3 Registers

Address Seen From Sound-CPU	Address Seen From SCPU	Register Name	W/R	Function Seen From Sound-CPU Section
00F4H	2140H	Port0r Port0w	R W	Read content of Port0r reg. Write to Port0w reg.
00F5H	2141H	Port1r Port1w	R W	Read content of Port1r reg. Write to Port1w reg.
00F6H	2142H	Port2r Port2w	R W	Read content of Port2r reg. Write to Port2w reg.
00F7H	2143H	Port3r Port3w	R W	Read content of Port3r reg. Write to Port3w reg.

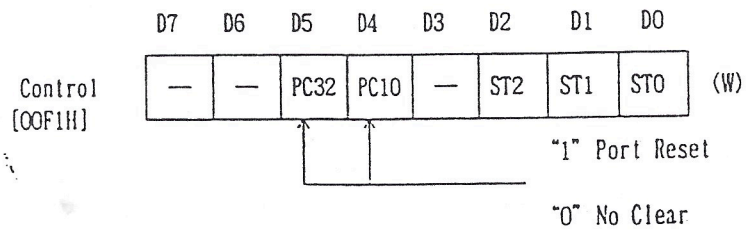
Fig. 2.2.1. I/O Diagram

3. CONTROL REGISTER

3.1. THE PORT CLEAR FUNCITON BY MEANS OF THE COANTROL REG.

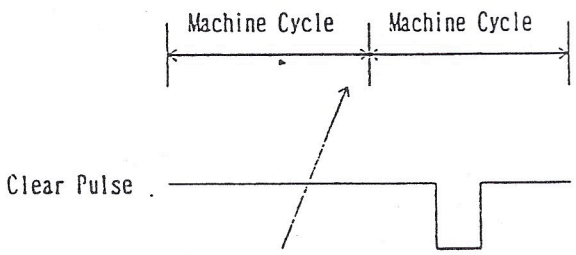
The ports are cleared to "00" when "1" is written into the Control register port clear control bits PC32. PCF10. When "0" is written in. they are not cleared.
When "1" is written into the port clear control bit PC10. both the port Or register and the port 1r register are cleared to "00". In the same manner, when "1" is written into PC32. both the port 2r register and the port 3r register are cleared to "00".

CONTROL REGISTER



When Reset: "--00-000"

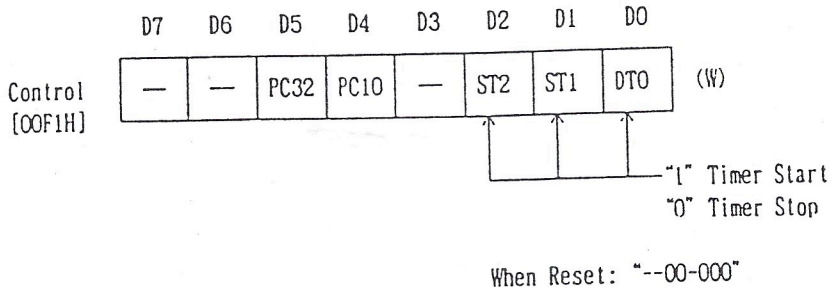
Note: Clear Timing
Port clear is executed during the machine cycle following that in which "1" is written into the port clear control bit.
When port clear timing conflicts with write timing to the port in question from the SFX bus. there are cases in which the contents of the register in question become indeterminate.



Timing when "1" is written into the port clear control bit.

3.2. TIMER CONTROL BY MEANS OF THE CONTROL REG.

CONTROL REGISTER



When Reset: "--00-000"

STO is the Timer TO start/stop control bit: the timer stops with "0" and starts with "1". At this timer. it is necessary to input "1" into STO once it has been changed to "0".
ST1 and ST2 are respectively the start/stop control bits of timers T1 and T2. Their function is identical to that of STO.

NOTE) In regard to the timers, please see next section.

4. TIMERS

4.1. FUNCTION OF TIMERS T0, T1, T2

The SFX sound source is provided with three timers, T0, T1, and T2.

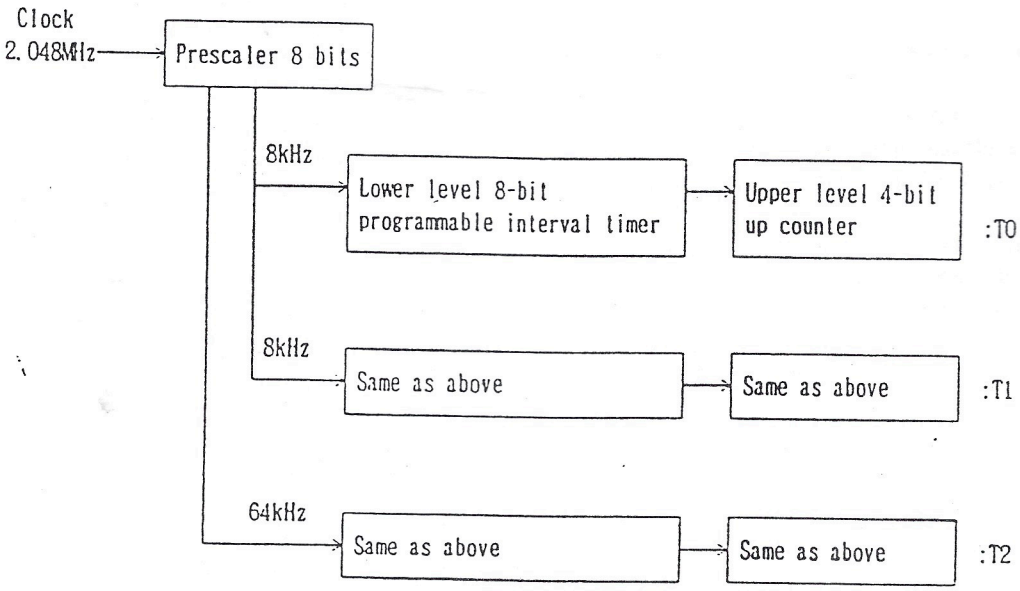


Fig. 4.1. Timer Section

The timers T0, T1, and T2 are each composed of a lower level 8-bit programmable interval timer connected to a upper level 4-bit up counter.
The 8-bit timer is made up of an 8-bit binary up counter, comparator, timer register and control circuit; and each of the timers T0, T1 and T2 is independently programmable.
The clock input to timers T0 and T1 from the prescaler is 8kHz (125 μs), and that to timer T2 from the prescaler is 64kHz (15.6 μs).

Table 4.1. Timer Function

	8-bit Timer		4-bit Up Counter
	Resolution	Max. Count Value	Max. Count Value
Timer T0, T1	125 μsec.	32msec.	512msec.
Timer T2	15.6 μsec.	4msec.	64msec.

4.2. TIMER ACTION

Since each timer T0, T1 and T2 is structured identically, explanation will be made taking timer T0 as an example.

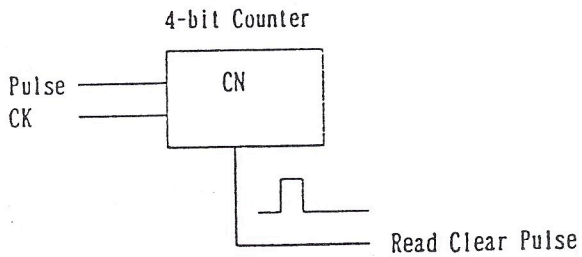
The lower level 8-bit timer of timer T0 is composed principally of a binary up counter, which is increamented at each count clock input. When its value corresponds to the contents of the timer register, it is cleared to 00H. Simultaneously a pulse is generated to the 4-bit up counter.

The 4-bit up counter is composed principally of a binary up counter, which increments at each input of a lower level pulse.

The action of the counter of timer T0 is controlled by the 0 bit of the control register. When bit ST0 is "0" count up is suspended. Count up commences when both upper level and lower level counters are cleared by "1". Consequestly, in order to clear the counters, it is necessary to set bit ST0 to "1" after having once set it to "0".

Writing into the timer register is carried out while the counter is stopped. At this time, the minimum value of the write value is 01H and the maximum value is 00H. Though it is not possible to read the value of the timer register, it is possible to read the 4-bit value CN0 at any time. When the value of CN0 is read, only the 4-bit up counter section is cleared to "00".

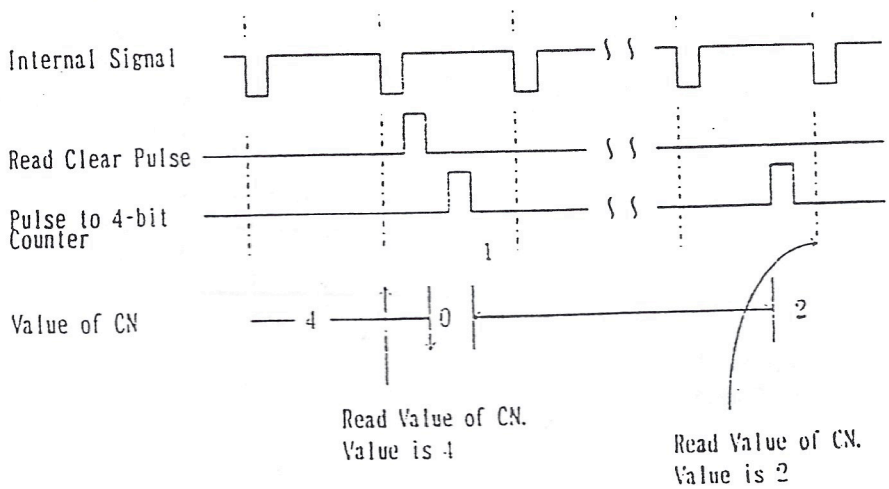
Upper Level 4-bit Counter Timing



Action of timer T0 is stopped by means of the reset input ($\overline{POR}$="L"). At this time of reset, ST0 of the control register is "0", and CN0 and TM0 of the timer register are indeterminate.

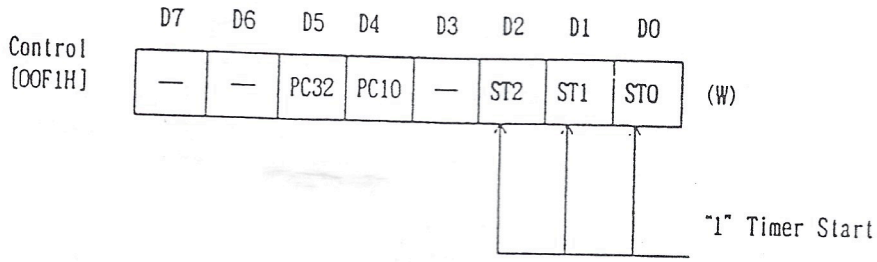
when CN is read, the 4-bit up counter alone is cleared through IC internal timing, but the read clear pulse and the pulse to the 4-bit up counter do not conflict with each other.

Consequently, when the pulse is input to the 4-bit up counter, the vlaue of CN will necessarily be incremented or when value of CN is read, CN will be cleared and CN will become "0".



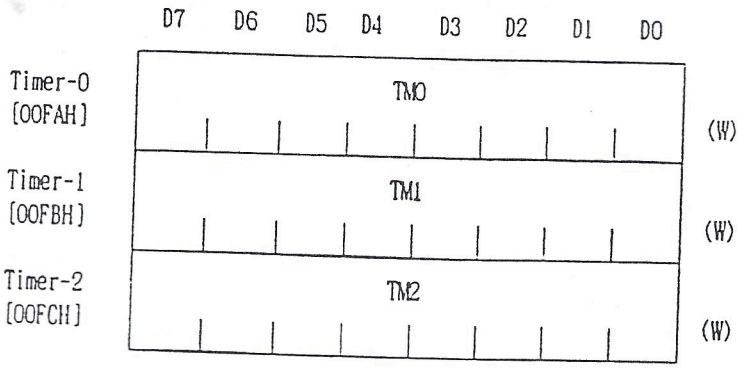
4.3. TIMER RELATED REGISTERS

Control Register

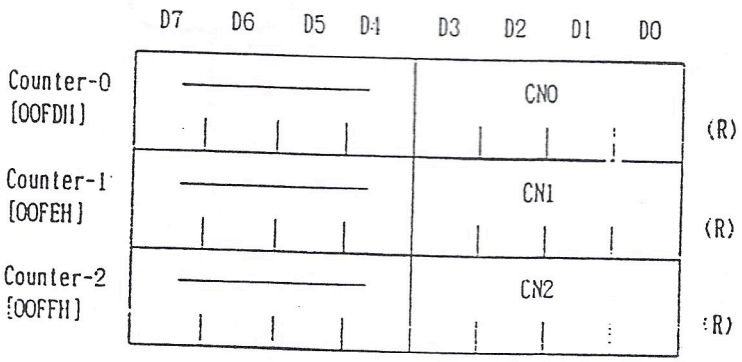


When Reset: "--00-000"

Timer Register



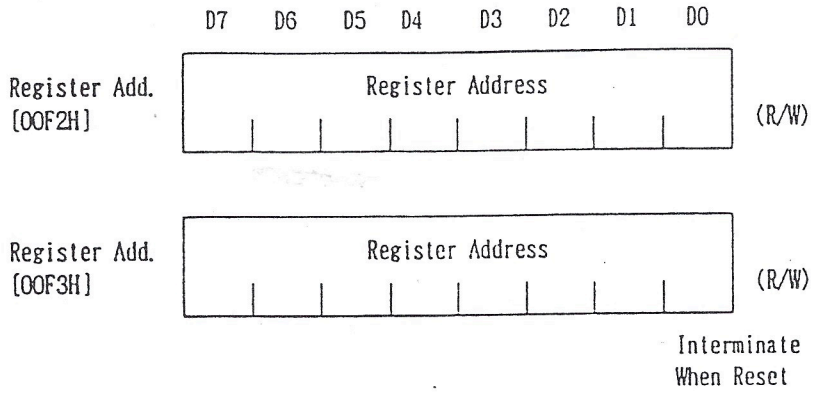
Counter Register



Interminate
When Reset

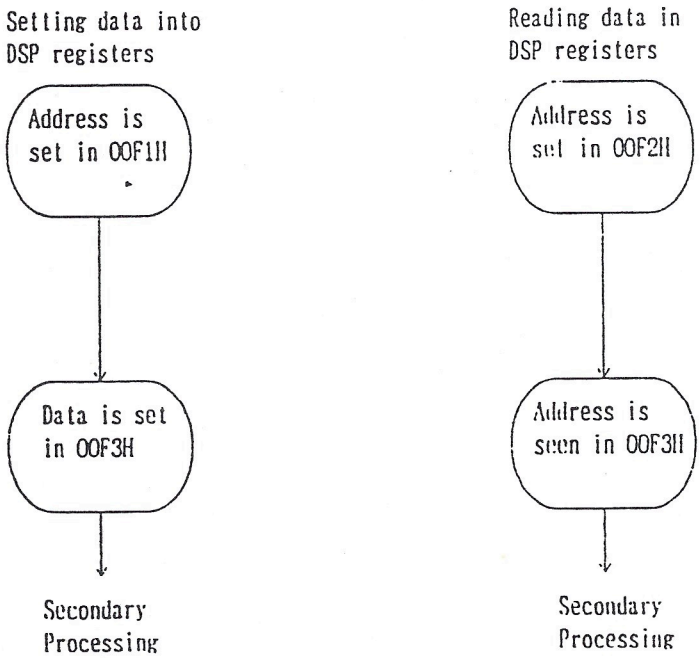
5. DSP INTERFACE REGISTER

Interface register



This is the register which sets data into the registers within DSP. Values are set into the designated register in accordindance with the course of the flow-chart below.

i) The DSP address to be set is written into 00F2H.
ii) Data is written into 00F3H.

When the content of the register data is to be read. it also follows the flow-chart below.

i) The address to be read if set in 00F2H.
ii) The content of 00F3H is seen.